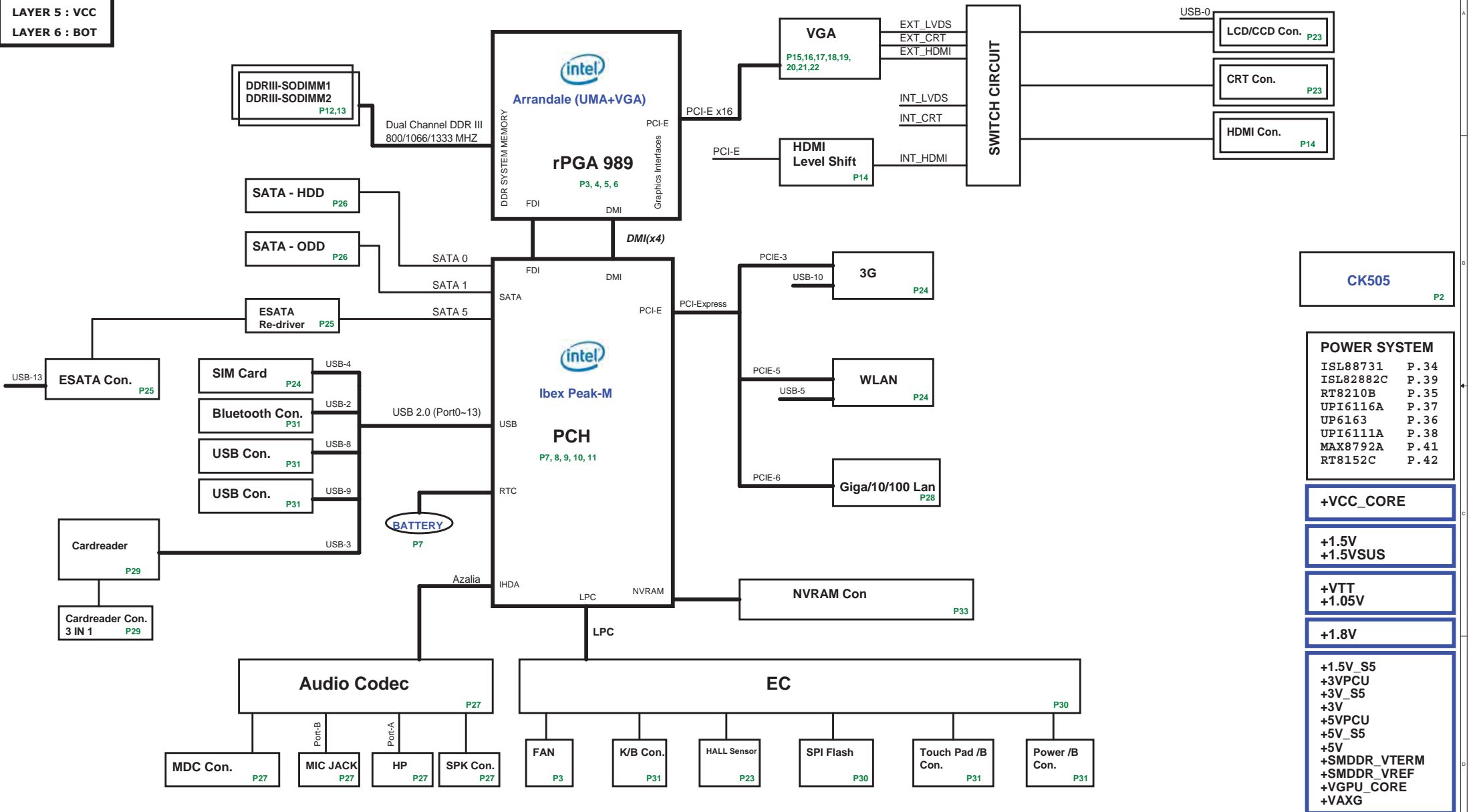


PCB STACK UP

- LAYER 1 : TOP
- LAYER 2 : GND
- LAYER 3 : IN1
- LAYER 4 : IN2
- LAYER 5 : VCC
- LAYER 6 : BOT

BL6 Block Diagram



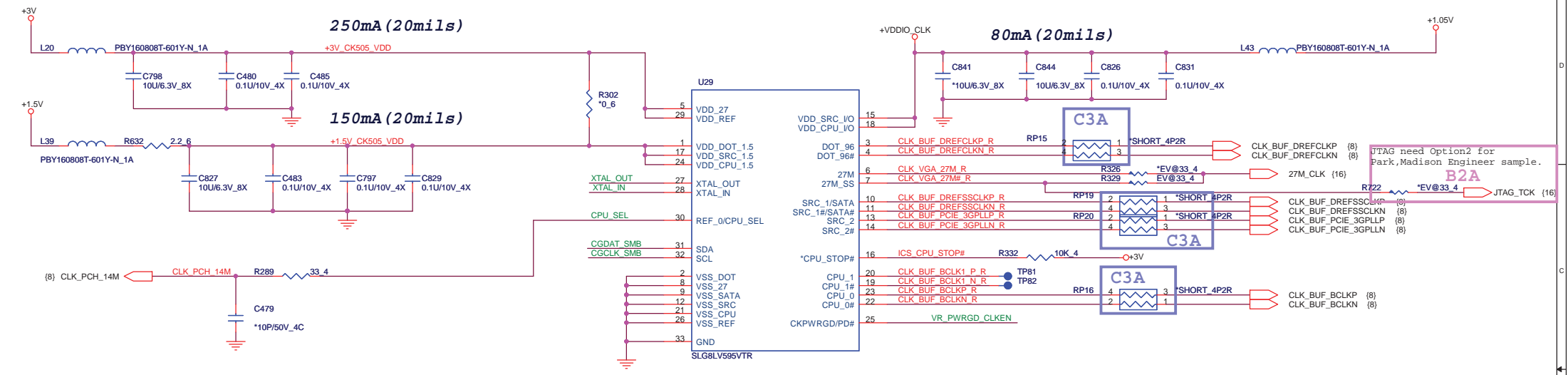
**POWER SYSTEM**

ISL88731	P.34
ISL82882C	P.39
RT8210B	P.35
UPI6116A	P.37
UP6163	P.36
UPI6111A	P.38
MAX8792A	P.41
RT8152C	P.42

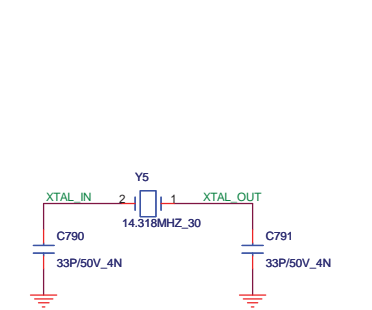
- +VCC\_CORE
- +1.5V
- +1.5VSUS
- +VTT
- +1.05V
- +1.8V
- +1.5V\_S5
- +3VPCU
- +3V\_S5
- +3V
- +5VPCU
- +5V\_S5
- +5V
- +SMDDR\_VTERM
- +SMDDR\_VREF
- +VGPU\_CORE
- +VAXG



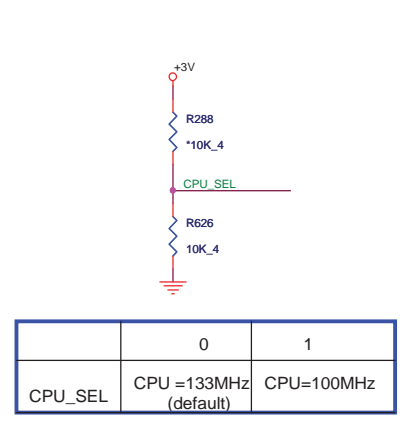
CLOCK Gen



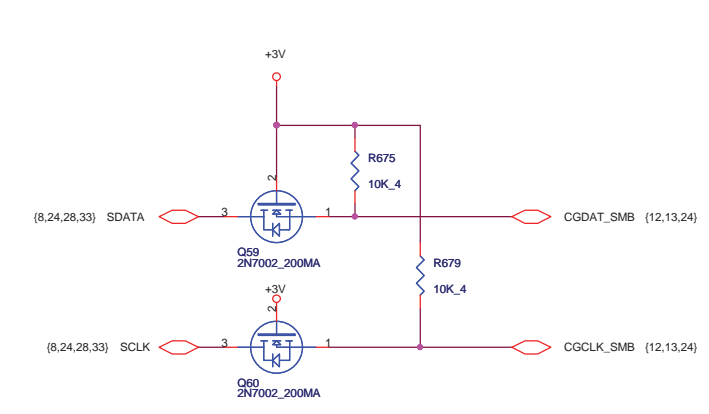
CLK CRYSTAL



CLK CPU\_SEL

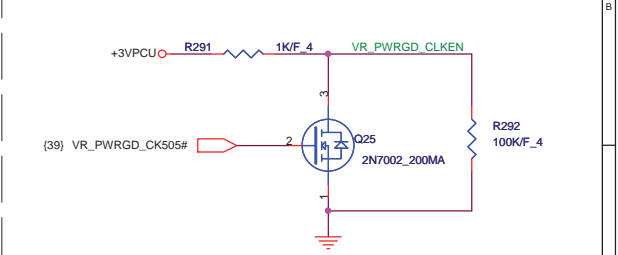



CLK I2C



CLK POWERGOOD

Change to +3VPCU (follow CRB)

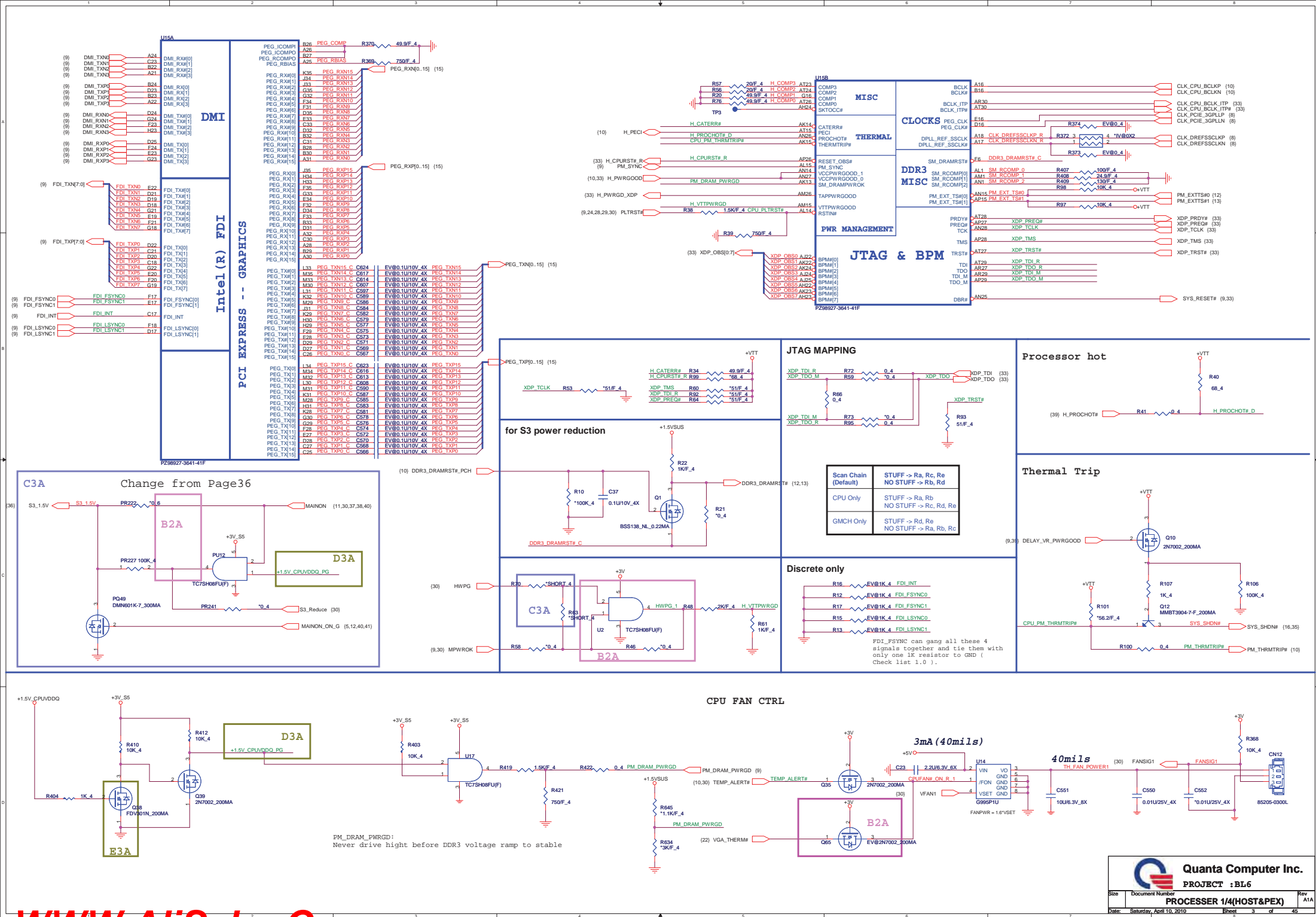




**Quanta Computer Inc.**  
**PROJECT : BL6**

Size	Document Number	Rev
	<b>CLOCK GENERATOR</b>	A1A
Date:	Thursday, April 06, 2010	Sheet 2 of 45









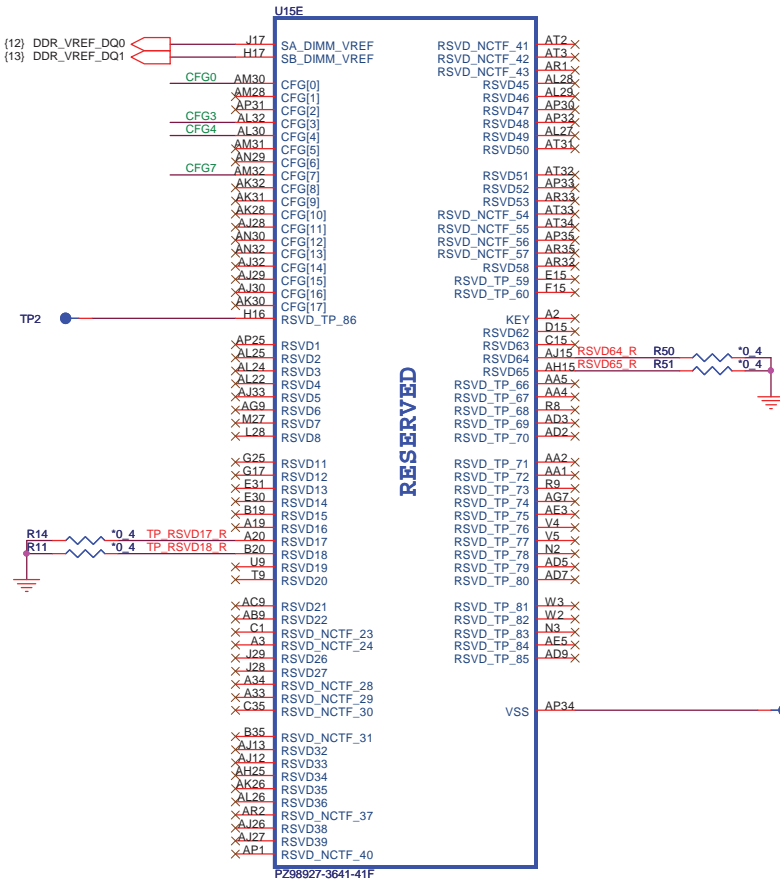
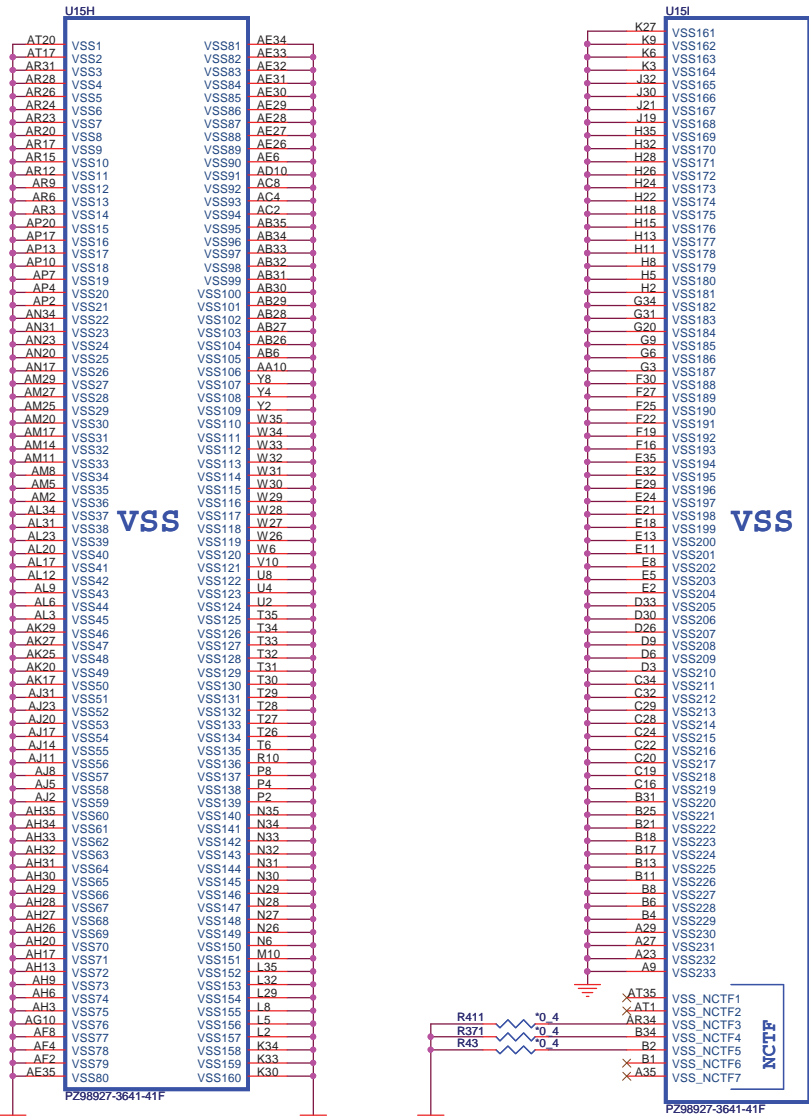






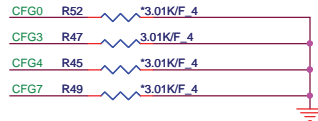
AUBURNDAL/CLARKSFIELD PROCESSOR (GND)

AUBURNDAL/CLARKSFIELD PROCESSOR( RESERVED, CFG)

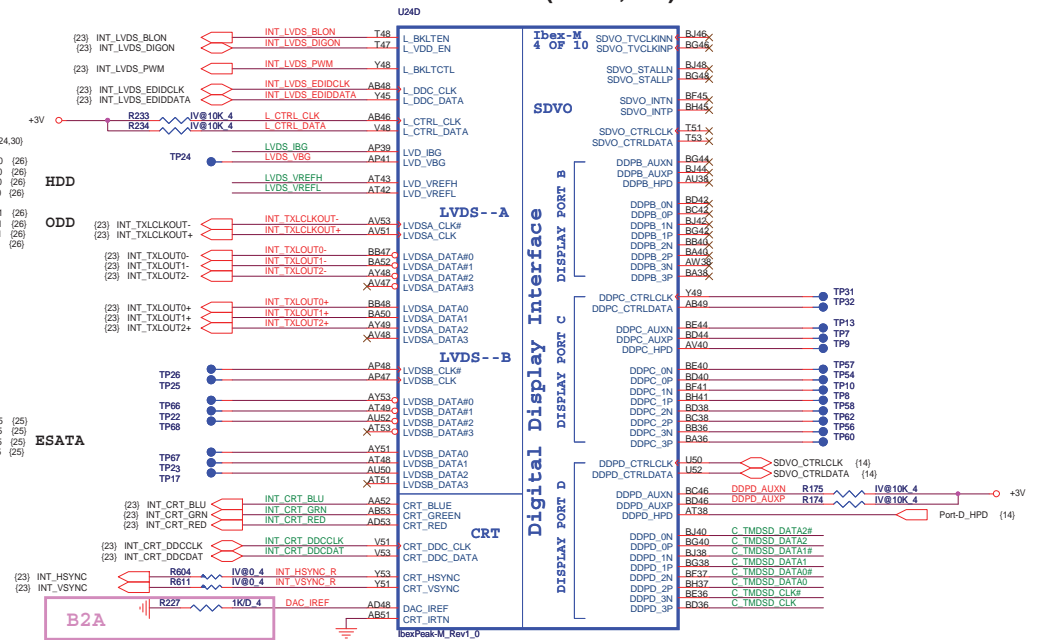
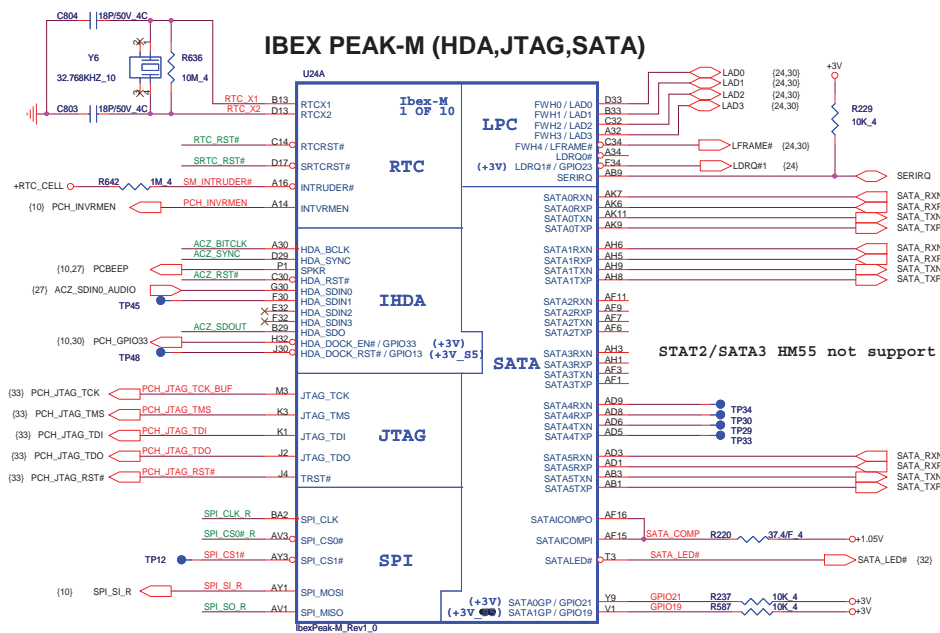


Processor Strapping

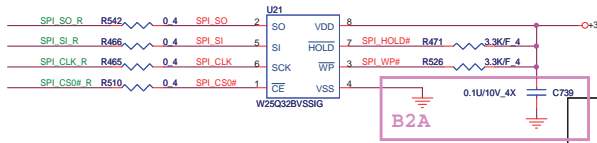
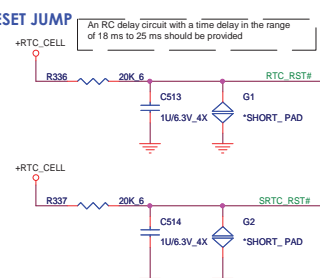
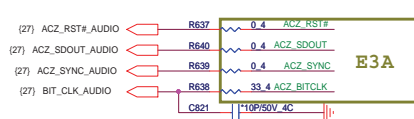
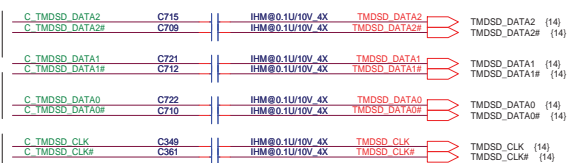
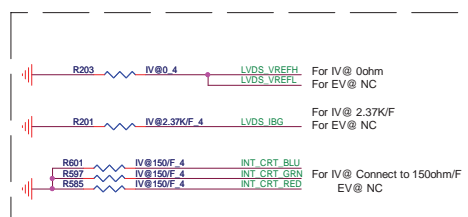
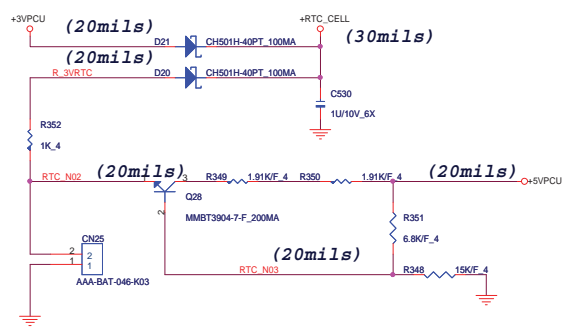
	1	0
CFG4 (Display Port Presence)	Disabled; No Physical Display Port attached to Embedded Display Port	Enabled; An external Display port device is connected to the Embedded Display port
CFG0 (PCI-Epress Configuration Select)	Single PEG	Bifurcation enabled
CFG3 (PCI-Epress Static Lane Reversal)	Normal Operation	Lane Numbers Reversed 15 -> 0 , 14 -> 1



















Port	Strap	How to enable Port?	How to disable Port?
LVDS	L_DDC_DATA	PU to 3.3V with 2.2k+/- 5%	NC
Port B	SDVO_CTRLDATA	PU to 3.3V with 2.2k+/- 5%	NC
Port C	DDPC_CTRLDATA	PU to 3.3V with 2.2k+/- 5%	NC
Port D	DDPD_CTRLDATA	PU to 3.3V with 2.2k+/- 5%	NC
eDP	CFG[4]	PD to GND directly	NC

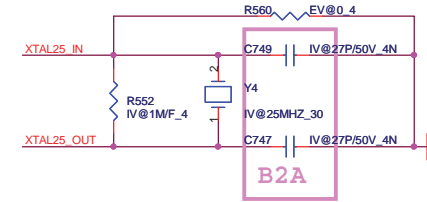
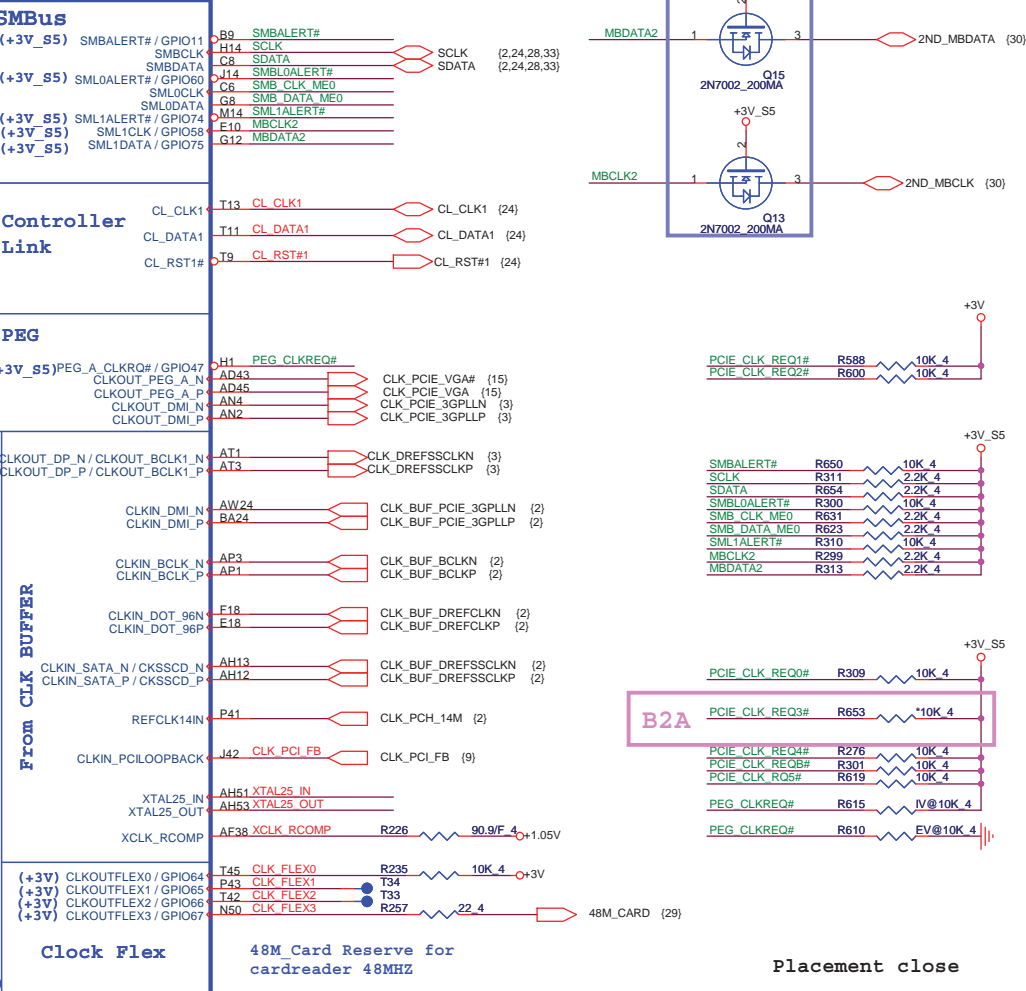
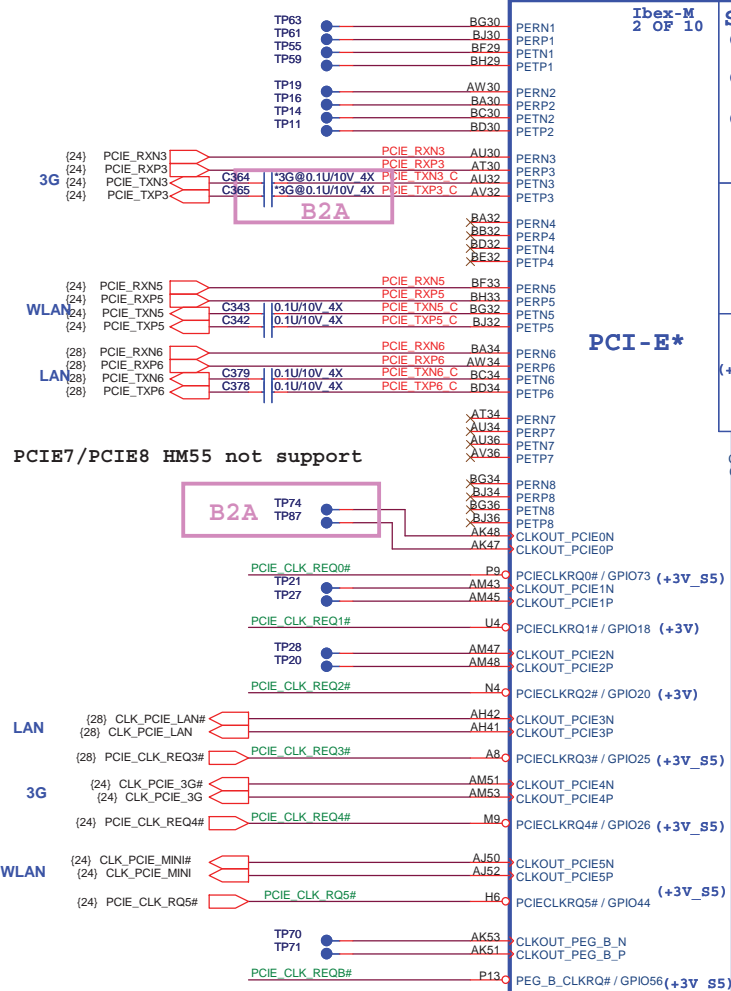


PCH	2MB	4MB	8MB
PM55			
HM55			
HM57/PM57			
QM57/QS57			



A17	VSS159	VSS259	H49
B11	VSS160	VSS260	H5
B15	VSS161	VSS261	J24
B19	VSS162	VSS262	K11
B23	VSS163	VSS263	K43
B27	VSS164	VSS264	K47
B35	VSS165	VSS265	K7
B39	VSS166	VSS266	K14
B43	VSS167	VSS267	L18
B47	VSS168	VSS268	L2
B7	VSS169	VSS269	L22
BG12	VSS170	VSS270	L32
BH12	VSS171	VSS271	L36
BH16	VSS172	VSS272	L40
BH20	VSS173	VSS273	L50
BH24	VSS174	VSS274	M12
BH30	VSS175	VSS275	M16
BH35	VSS176	VSS276	M20
BH38	VSS177	VSS277	N38
BH42	VSS178	VSS278	M34
BH49	VSS179	VSS279	M38
BH5	VSS180	VSS280	M42
BC14	VSS181	VSS281	M46
BC18	VSS182	VSS282	M5
BC2	VSS183	VSS283	M9
BC22	VSS184	VSS284	N24
BC22	VSS185	VSS285	M8
BC32	VSS186	VSS286	P11
BC34	VSS187	VSS287	AD15
BC40	VSS188	VSS288	P22
BC44	VSS189	VSS289	P30
BC52	VSS190	VSS290	P32
BH9	VSS191	VSS291	P34
BD48	VSS192	VSS292	P42
BD49	VSS193	VSS293	P47
BD5	VSS194	VSS294	R2
BE12	VSS195	VSS295	R12
BE20	VSS196	VSS296	R52
BE24	VSS197	VSS297	T29
BE24	VSS198	VSS298	T41
BE30	VSS199	VSS299	T46
BE34	VSS200	VSS300	T49
BE38	VSS201	VSS301	T5
BE42	VSS202	VSS302	T8
BE46	VSS203	VSS303	U30
BE48	VSS204	VSS304	U31
BE50	VSS205	VSS305	U32
BE6	VSS206	VSS306	U34
BE8	VSS207	VSS307	P38
BF3	VSS208	VSS308	P11
BF49	VSS209	VSS309	V16
BF51	VSS210	VSS310	V20
BG18	VSS211	VSS311	V22
BG24	VSS212	VSS312	V30
BH11	VSS213	VSS313	V31
BH15	VSS214	VSS314	V30
BH15	VSS215	VSS315	V32
BH15	VSS216	VSS316	V34
BH15	VSS217	VSS317	V35
BH23	VSS218	VSS318	V43
BH31	VSS219	VSS319	V48
BH35	VSS220	VSS320	V45
BH39	VSS221	VSS321	V46
BH43	VSS222	VSS322	V49
BH7	VSS223	VSS323	V5
C12	VSS224	VSS324	V7
C22	VSS225	VSS325	V8
C50	VSS226	VSS326	V8
D51	VSS227	VSS327	W2
E12	VSS228	VSS328	W52
E16	VSS229	VSS329	Y11
E20	VSS230	VSS330	Y12
E24	VSS231	VSS331	Y15
E30	VSS232	VSS332	Y19
E34	VSS233	VSS333	Y28
E38	VSS234	VSS334	Y30
E42	VSS235	VSS335	Y32
E46	VSS236	VSS336	Y32
E48	VSS237	VSS337	Y38
E6	VSS238	VSS338	Y38
E8	VSS239	VSS339	Y43
F40	VSS240	VSS340	Y46
F5	VSS241	VSS341	P49
G10	VSS242	VSS342	Y6
G14	VSS243	VSS343	Y5
G18	VSS244	VSS344	Y8
G2	VSS245	VSS345	P24
G22	VSS246	VSS346	T43
G32	VSS247	VSS347	AD51
G36	VSS248	VSS348	AD7
G40	VSS249	VSS349	Y47
G44	VSS250	VSS350	AT8
G48	VSS251	VSS351	AT12
AF39	VSS252	VSS352	AM6
E16	VSS253	VSS353	AT13
H20	VSS254	VSS354	AM5
H30	VSS255	VSS355	AK45
H34	VSS256	VSS356	AK39
H38	VSS257	VSS357	AV14
H42	VSS258		

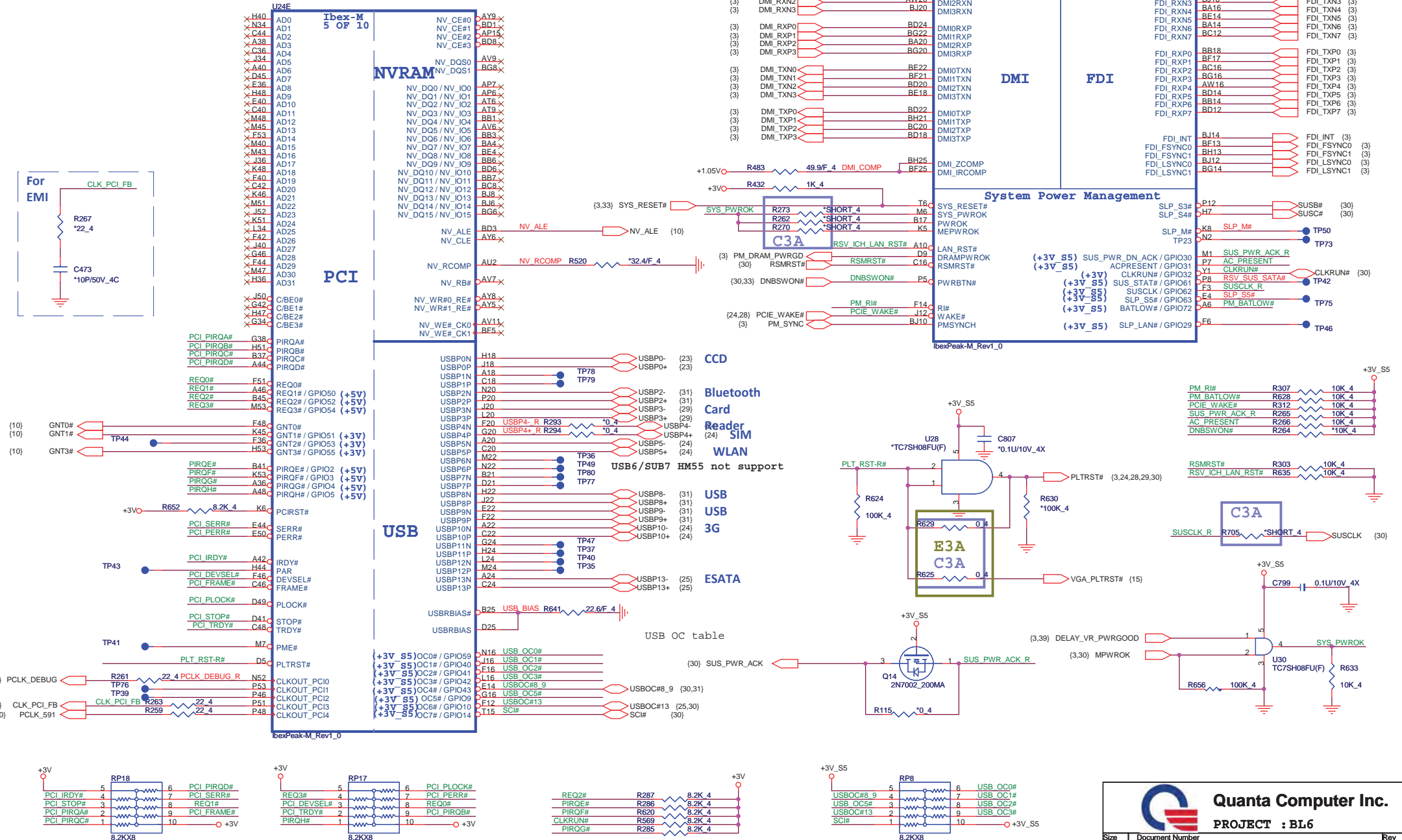
## U24B





## IBEX PEAK-M (DMI,FDI,GPIO)

## IBEX PEAK-M (PCI,USB,NVRAM)






## IBEX PEAK-M (GPIO,VSS\_NCTF,RSVD)

## IBEX PEAK-M (GND)

## PCH Strap Pin Configuration Table

## SPKR

(7,27) PCBEEP  R592 \*1K\_4 +3V


Reboot option at power-up  
0 = Default Mode (Internal weak Pull-down)  
1 = No Reboot Mode with TCO Disabled

GNT3#/  
GPIO55

(9) GNT3#  R622 \*10K\_4 +3V

Top-Block Swap Override  
0 = Top Block Swap Mode  
1 = Default Mode (Internal pull-up)

HDA\_DOCK\_EN  
#GPIO33

(7,30) PCH\_GPIO33  R282 \*1K\_4 +3V

Flash Descriptor Security Override  
0 = Flash Descriptor Security will be overridden  
1 = Security measure defined in the Flash Descriptor will be enabled.


GNT0#,  
GNT1#

(9) GNT0#  R272 \*1K\_4 +3V

(9) GNT1#  R621 \*1K\_4 +3V


Boot BIOS Strap		
PCI_GNT0#	GNT#1	Boot BIOS Location
0	0	LPC
0	1	PCI
1	0	Reserved (NAND)
1	1	SPI

## SPI\_MOSI

(7) SPI\_SI\_R  R504 \*1K\_4 +3V

TPM Functionality Disable  
1 = Enabled  
0 = Disable

## NV\_ALE

(9) NV\_ALE  R496 \*10K\_4 +1.8V


IntelR Anti-Theft Technology HDD Data Protection (Intel AT-d) Enable  
1 = Enabled  
0 = Disabled (Default)

## GPIO8

 R298 \*10K\_4 +3V\_S5

Reserved  
This signal has a weak internal pull up.  
NOTE: This signal should not be pulled low

## GPIO15

 R248 \*1K\_4 +3V\_S5

Reserved  
0 = Intel ME Crypto Transport Layer Security (TLS) cipher suite with no confidentiality  
1 = Intel ME Crypto Transport Layer Security (TLS) cipher suite with confidentiality

## GPIO27

 R232 \*10K\_4 +3V

On-Die PLL Voltage Regulator  
0 = Disables the Vcc/VRM. Need to use on-board filter circuits for analog rails.  
1 = Enables the internal Vcc/VRM to have a clean supply for analog rails. No need to use on-board filter circuit.  
This signal has a weak internal pull-up.

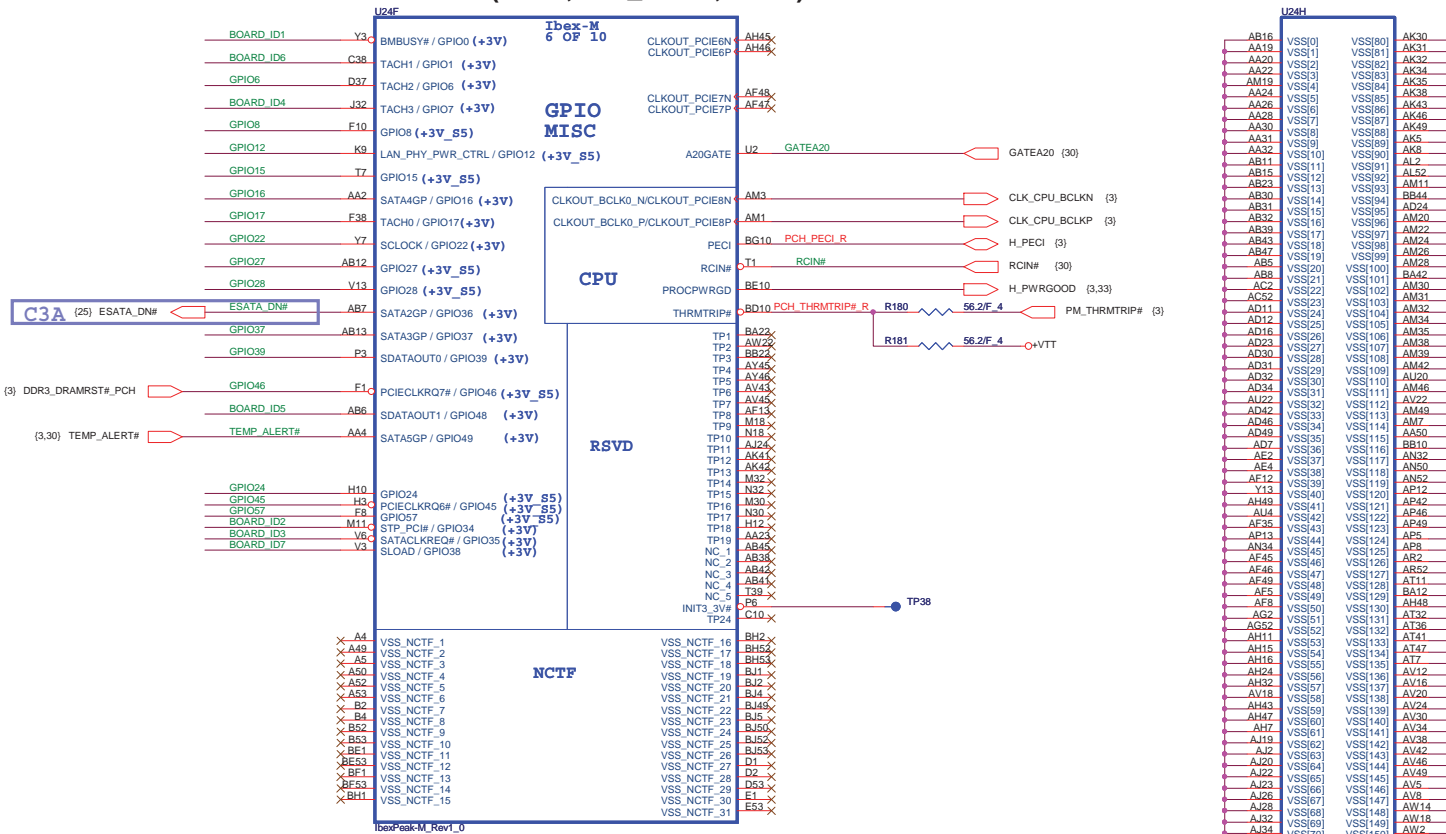
+RTC\_CELL  R644 \*330K\_6 PCH\_INVRMEN (7) PCH\_INVRMEN

INTVRMEN - Integrated SUS 1.1V VRM Enable  
High - Enable Internal VRs



Quanta Computer Inc.  
PROJECT : BL6

Size Document Number  
PCH 4/5 (GPIO & Strap)  
Date: Saturday, April 10, 2010 Sheet 10 of 45

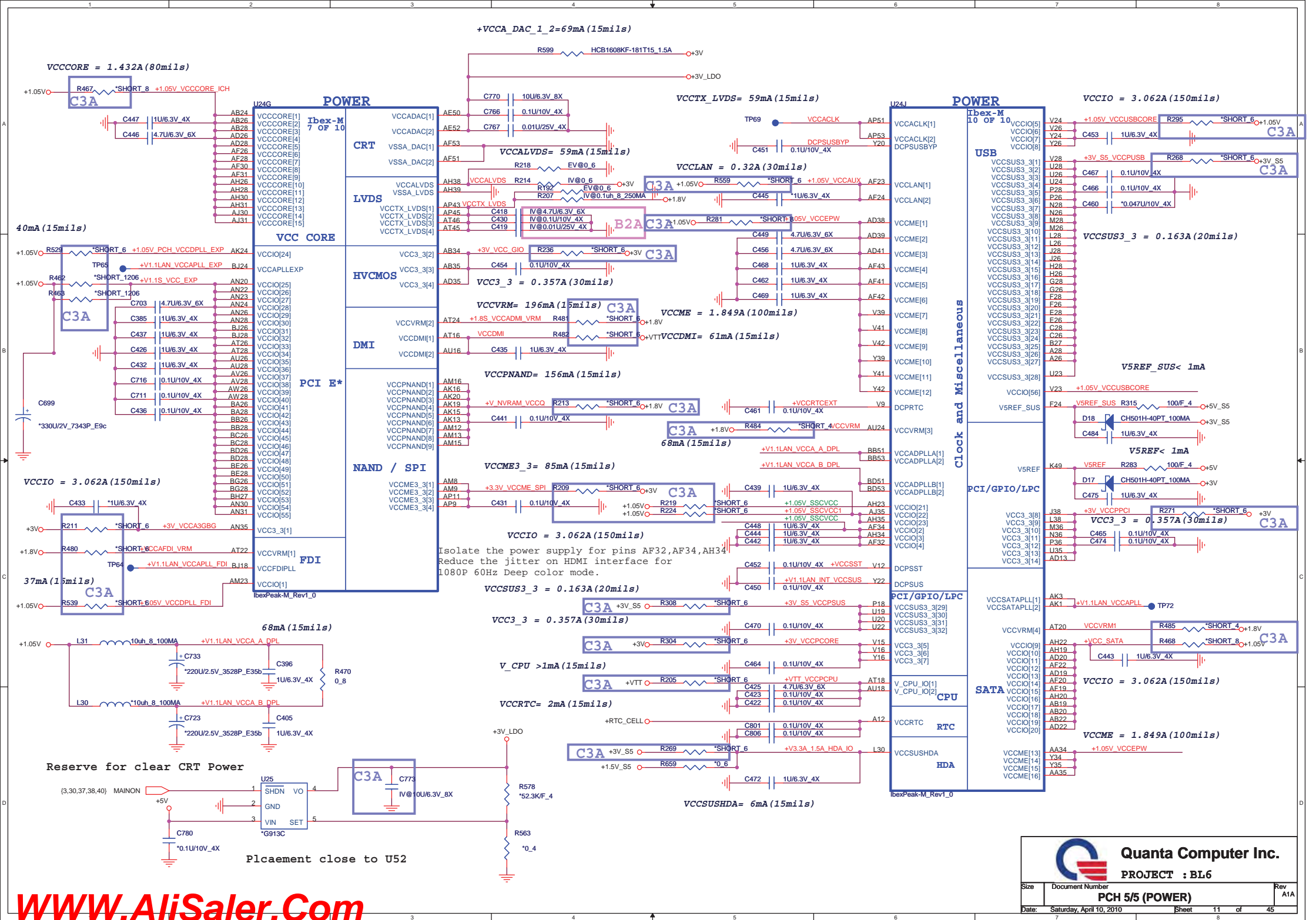


## BOARD ID SETTING

Board ID	ID1	ID2	ID3	ID4	ID5	ID6	ID7
UMA SKU	H	L					
VGA SKU							
W/ MDC			H	L			
W/O MDC							
W/ HDMI			H	L			
W/O HDMI							
W/O 3G					H	L	
W/ 3G							
15"							
14"					H	L	
W/O BT							H
W/ BT							L

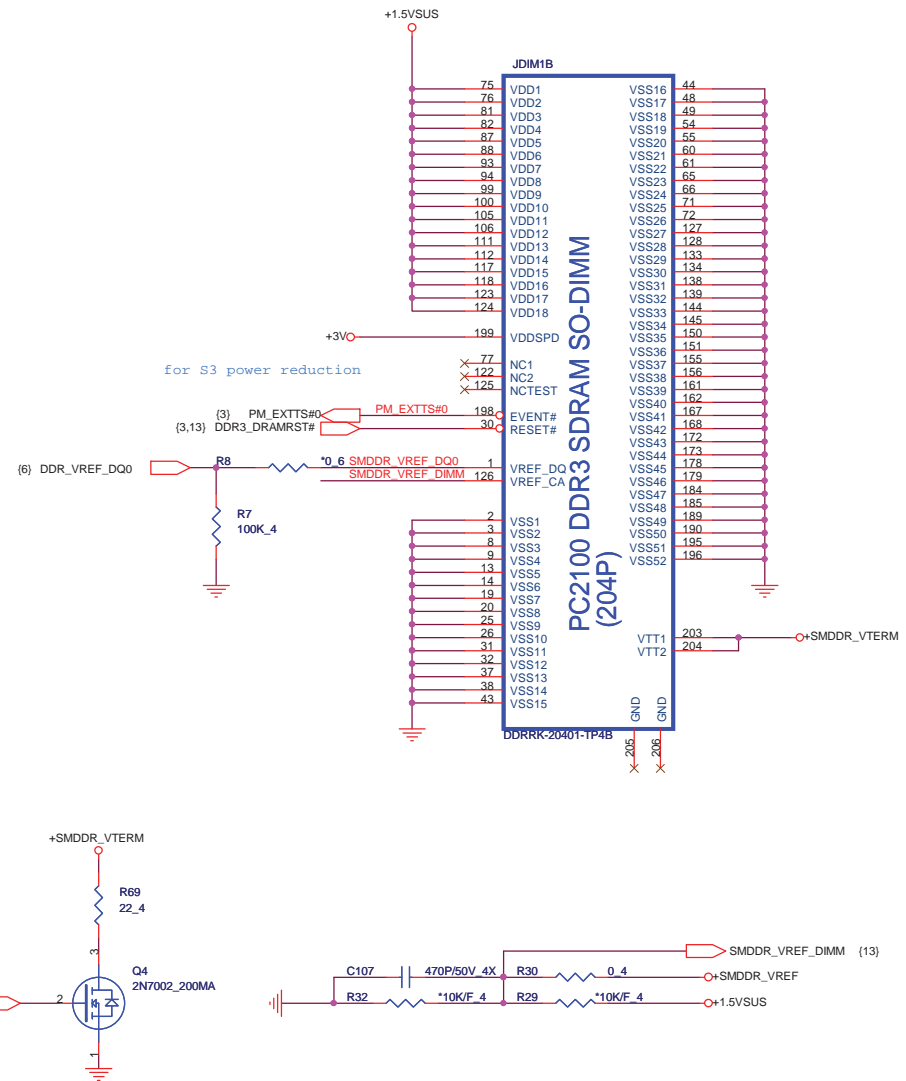
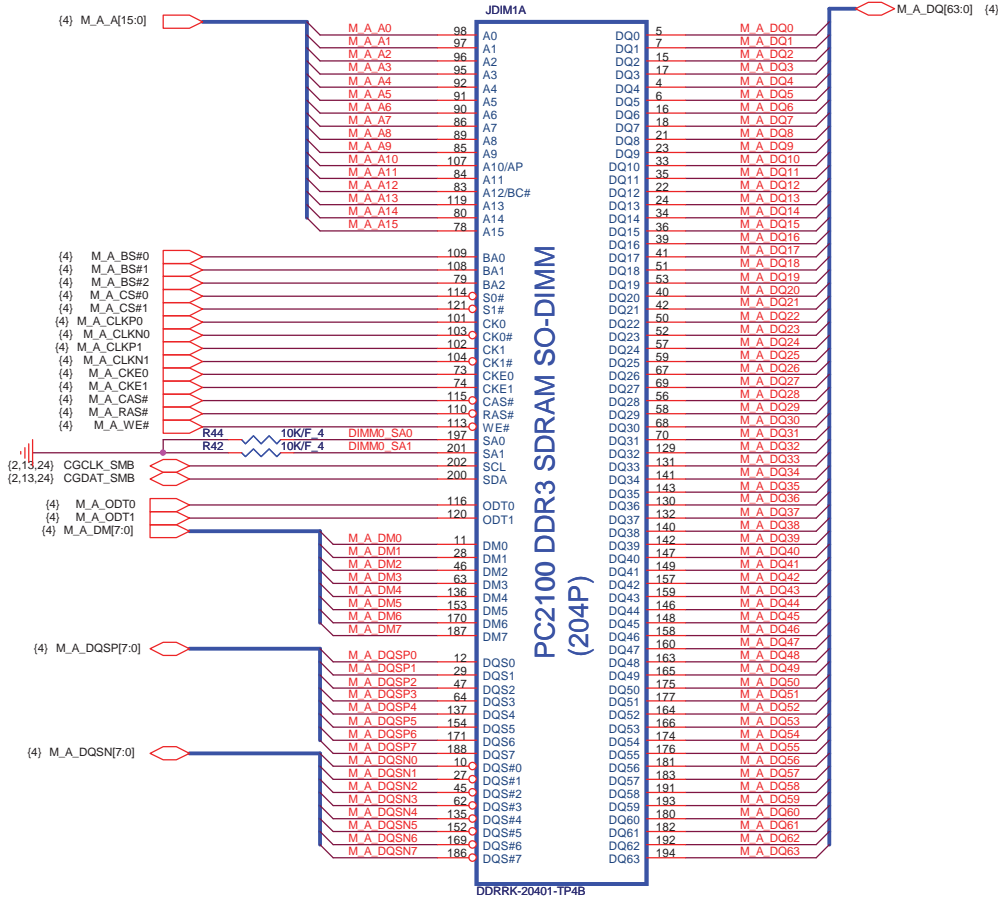
WWW.AliSaler.Com



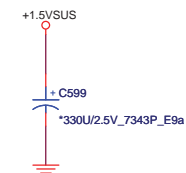
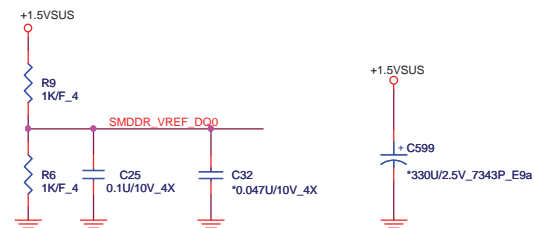
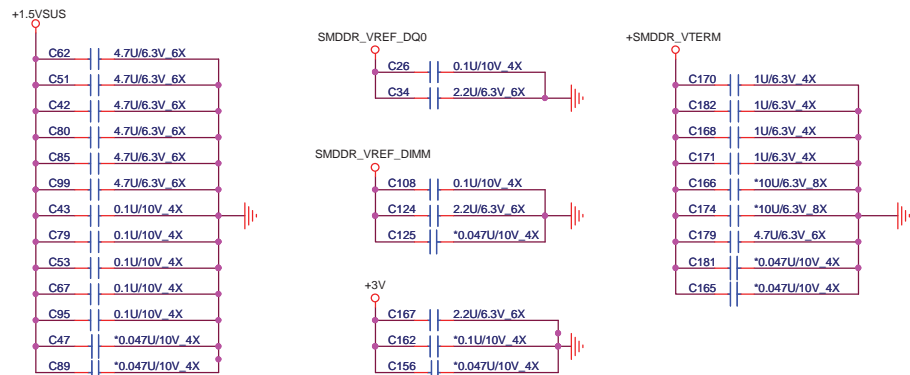




H=4



*Place these Caps near So-Dimm0.*

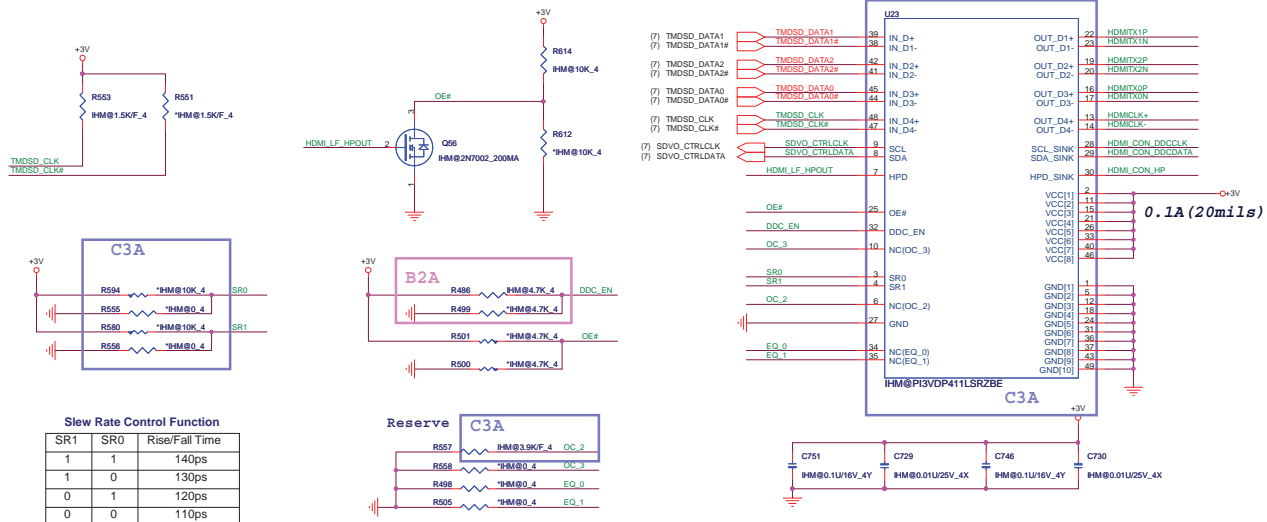




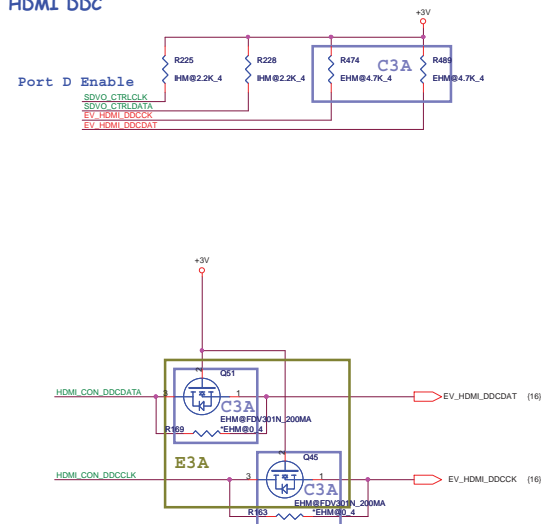




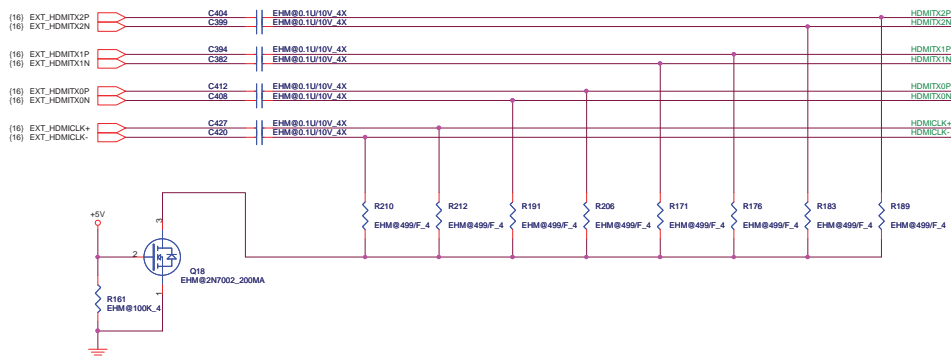
## HDMI Level Shift



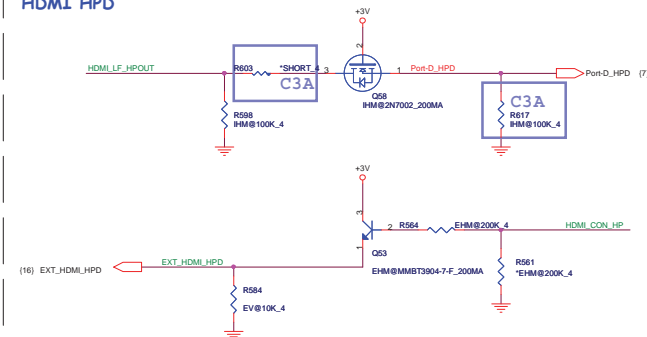
## HDMI DDC



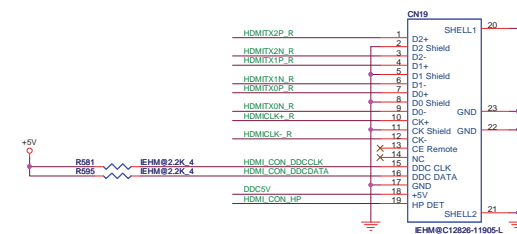
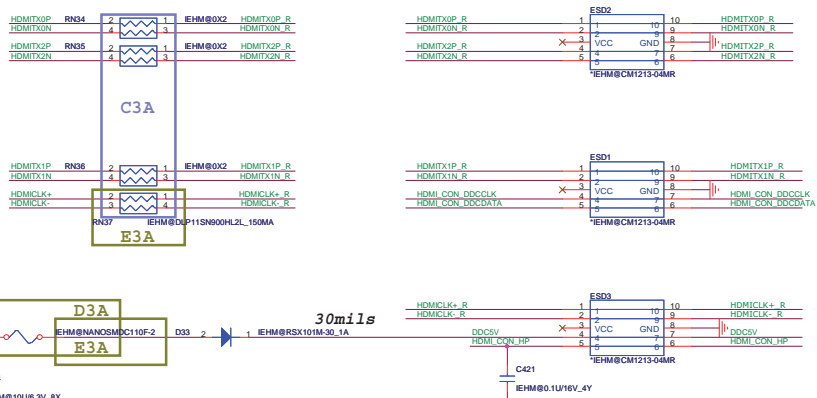
## Discrete HDMI



## HDMI HPD



Close to HDMI CONN









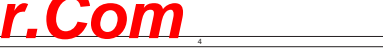
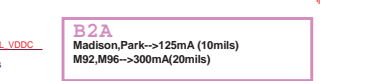
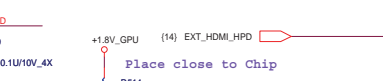
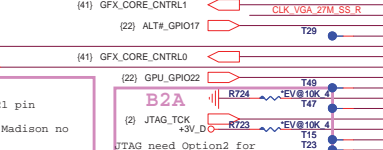
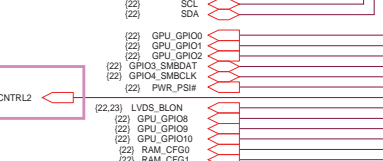
B2A

## JTAG SIGNAL STUFF OPTION FOR OPTION2

SIGNALS	NORMAL MODE	JTAG MODE (DEBU
TESTEN	"1" (PU)	"1" (PU)
GPIO24_TRSTB	"0" (PD)	"1" (PU)
GPIO26_TCK	CLK	"1" (PU)
GPIO27_TMS	"1" (PU)	"1" (PU)

1.8V GPIO

SCL must be tied high if not used



U20B

MUT1 GFX

DPA

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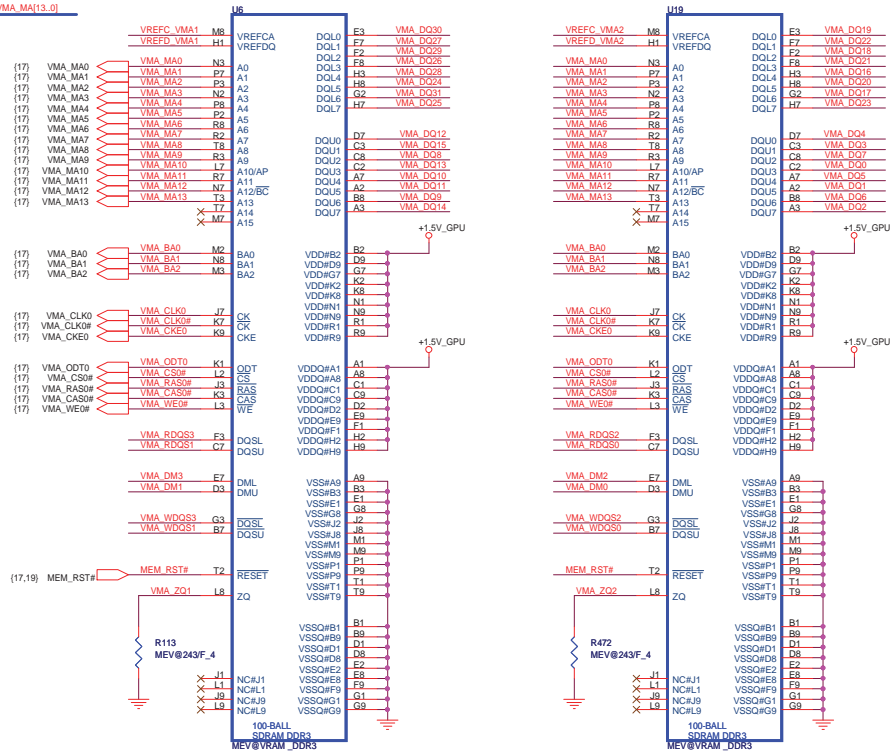




# CHANNEL A: 512MB DDR3 (64M\*16\*4pcs)

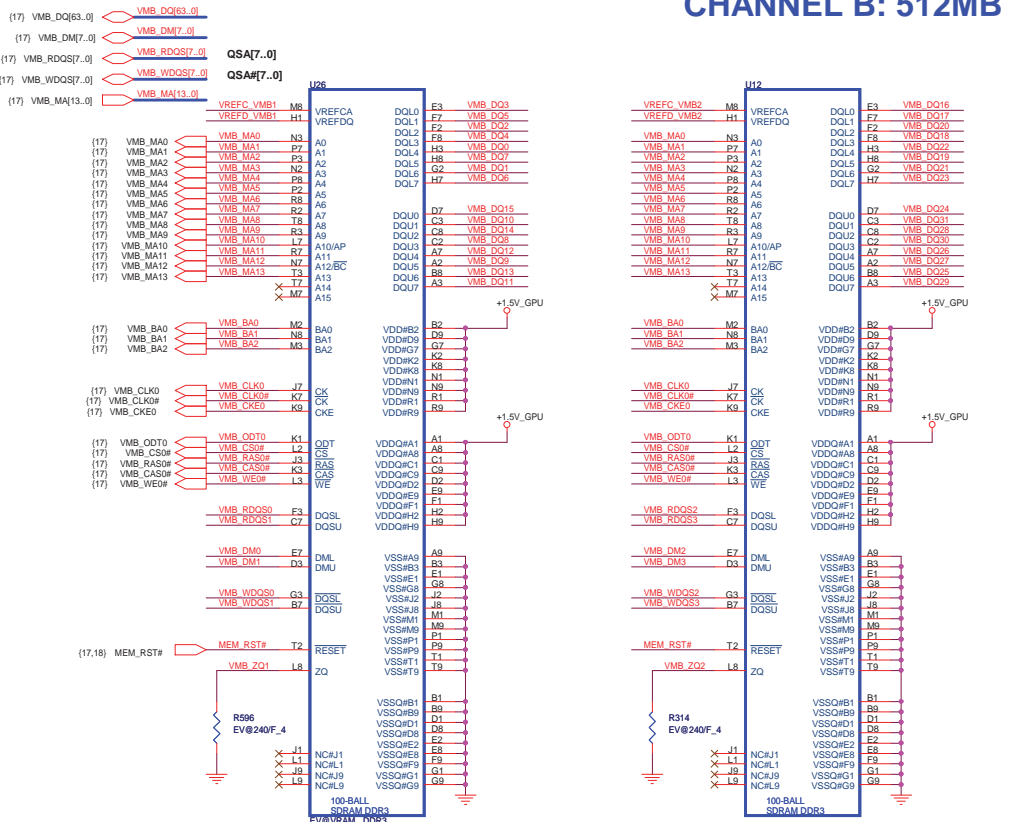
(17) VMA\_DQ[63..0] VMA\_DQ[63..0]  
 (17) VMA\_DM[7..0] VMA\_DM[7..0]  
 (17) VMA\_RDQS[7..0] VMA\_RDQS[7..0]  
 (17) VMA\_WDQS[7..0] VMA\_WDQS[7..0]  
 (17) VMA\_MA[13..0] VMA\_MA[13..0]

QSA[7..0]  
 QSA#[7..0]



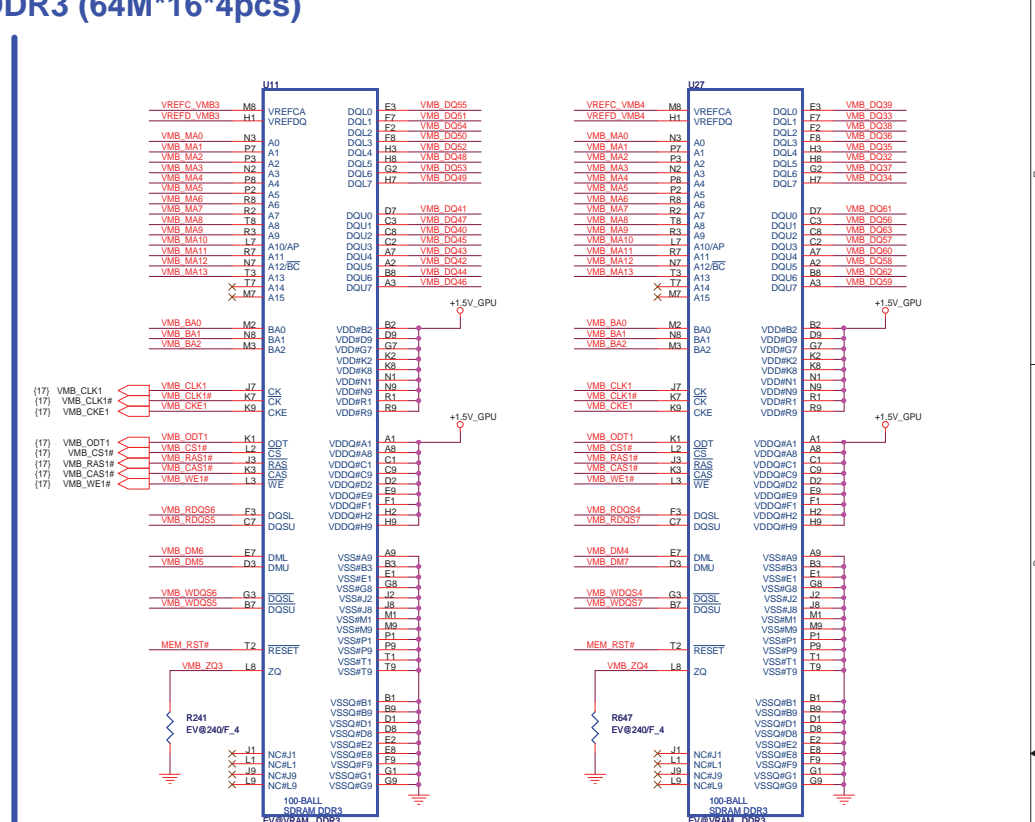


# CHANNEL B: 512MB DDR3 (64M\*16\*4pcs)



BOT Down

TOP Down

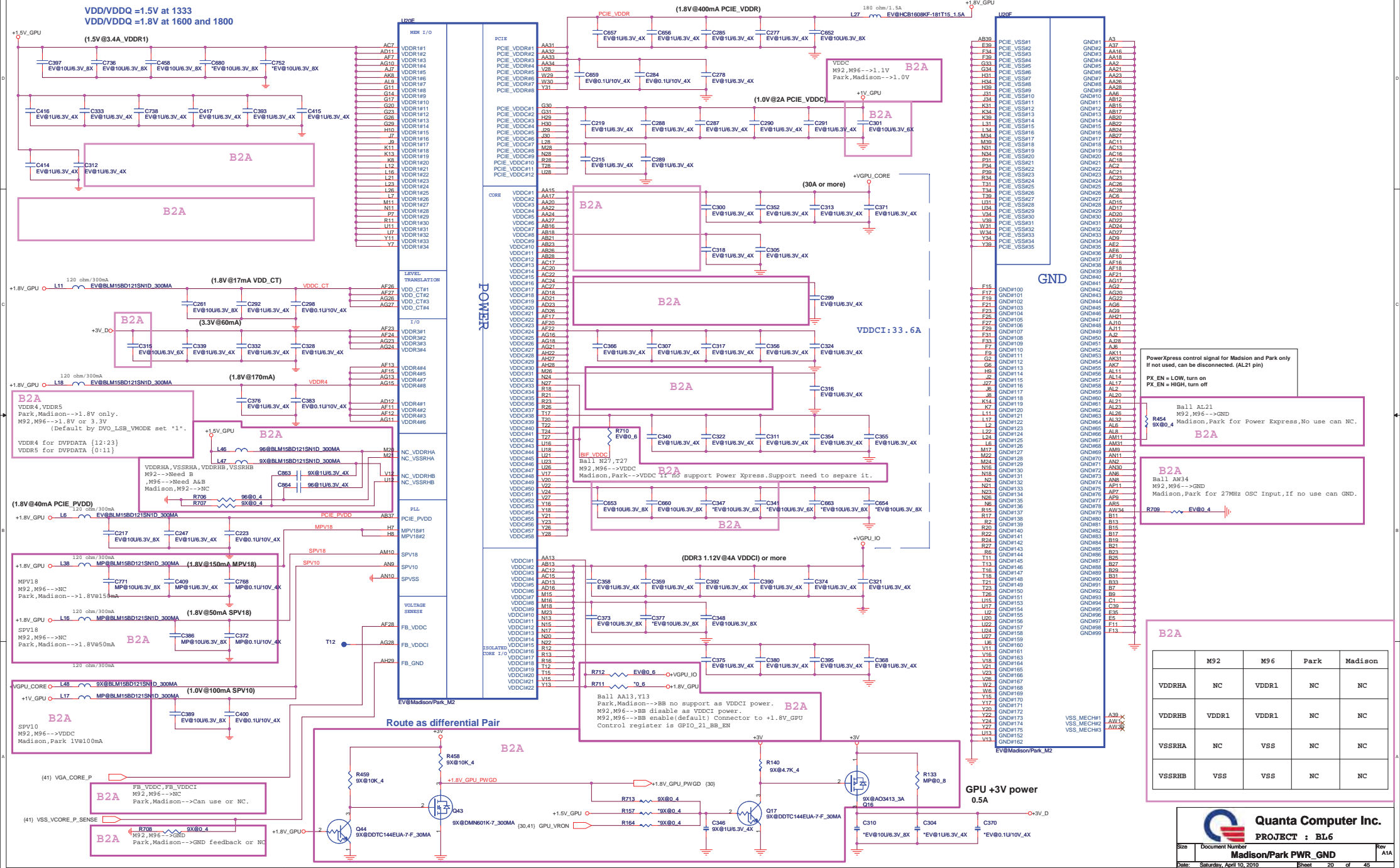


TOP Up

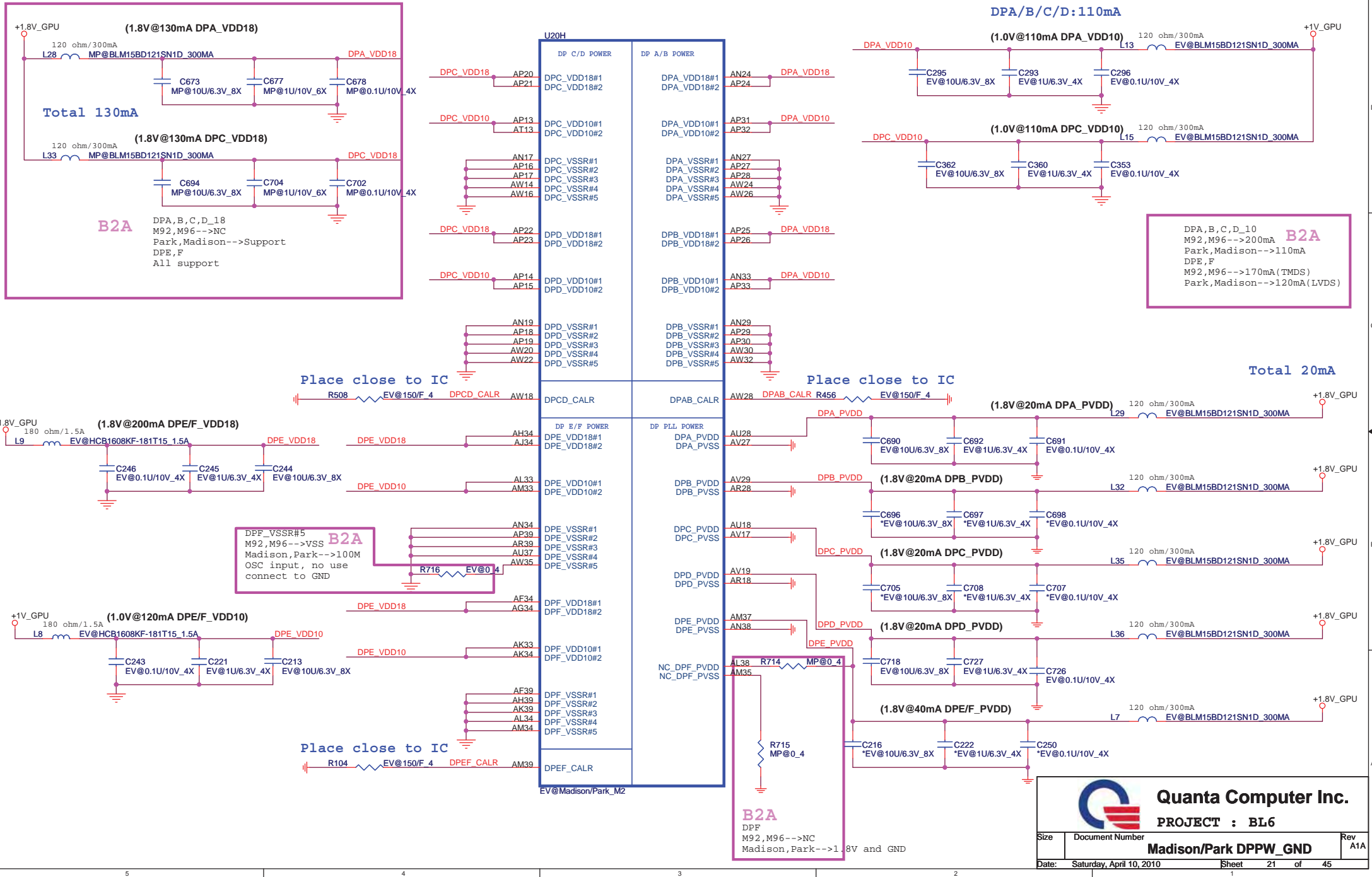
BOT Up



For Madison and Park VDDCI and VDDC can share one common regulator

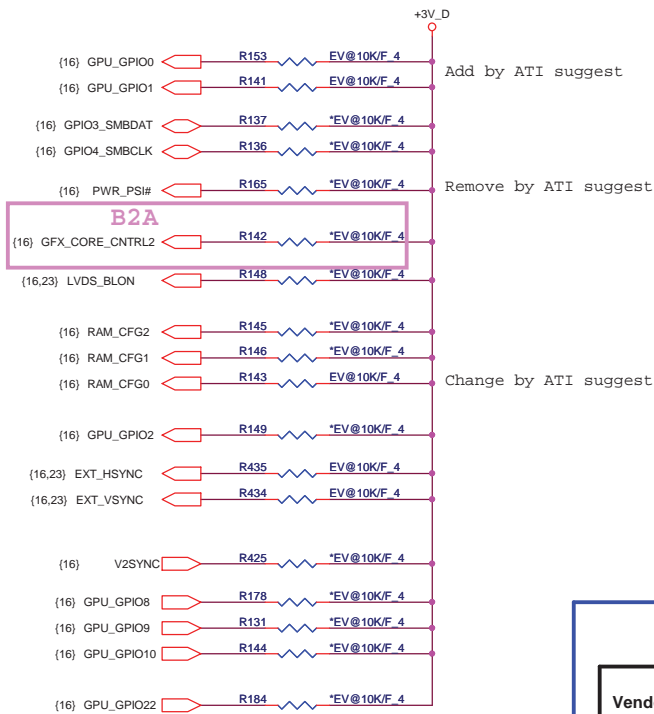








## PIN STRAPS



Memory Aperture size	
RAM_CFG[2:0]	Size
000	128MB
001	256MB
010	64MB
011	32MB

ROM Table		
EXT_HSYNC	EXT_VSYNC	Discription
0	0	No Audio
0	1	Any one by detect
1	0	DP only
1	1	Both DP & HDMI

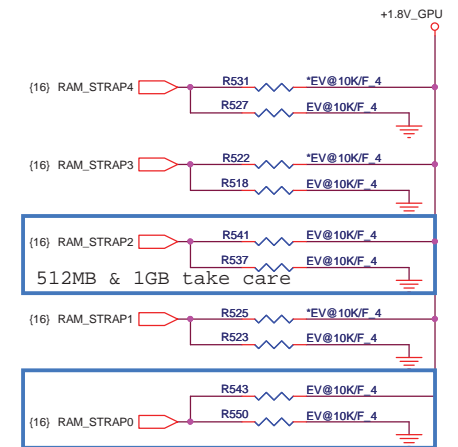
## CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET

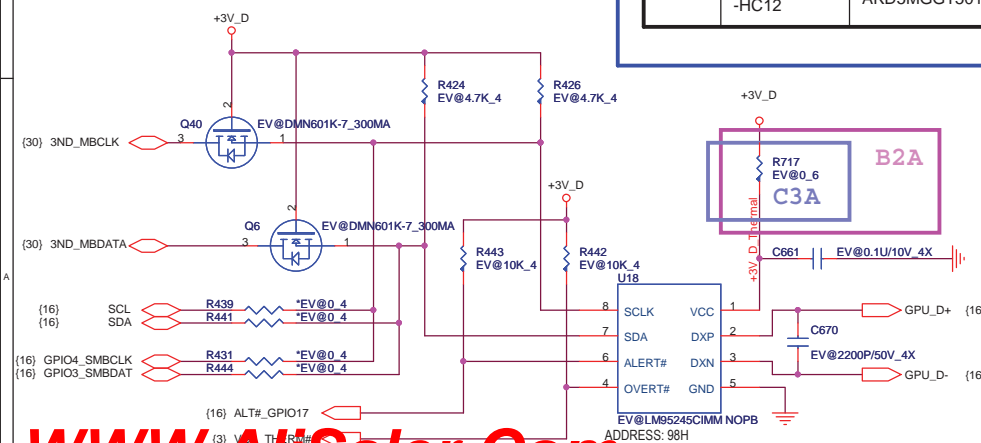
STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	DEFAULT	REMARK
TX_PWRS_ENB	GPIO0	0 = 50% TX OUTPUT SWING 1 = FULL TX OUTPUT SWING	0	
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED 0 = TX DE-EMPHASIS DISABLED 1 = TX DE-EMPHASIS ENABLED	0	
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM (Only for GDDR5) 0 = DISABLE 1 = ENABLE	0	
ROMIDCFG(2:0)	GPIO[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT NUMONYX M25P10A : 101	000	See ROM table
BIF_GEN2_EN_A	GPIO2	0 = PCIE DEVICE AS 2.5GT/S CAPABLE 1 = PCIE DEVICE AS 5GT/S CAPABLE	0	
GPIO_8_ROMSO H2SYNC GPIO_21_BB_EN	GPIO8 H2SYNC GPIO21	Reserved Only	0	
AUD[1] AUD[0]	HSYNC VSYNC	AUD[1:0] 00: NO AUDIO FUNCTION. 01: AUDIO FOR DISPLAYPORT AND HDMI IF ADAPTER IS DETECTED. 10: AUDIO FOR DISPLAYPORT ONLY. 11: AUDIO FOR BOTH DISPLAYPORT AND HDMI.	11	See Audio table
GPIO_9_ROMSI	GPIO9	0 = VGA controller capacity enable	0	
VIP_DEVICE_STRAP_ENA VIP: Video Capture Port Interface	V2SYNC	0 = DRIVER would ignore the value sample on VHAD_0 during RESET.	0	

## DDR3 Memory TYPE

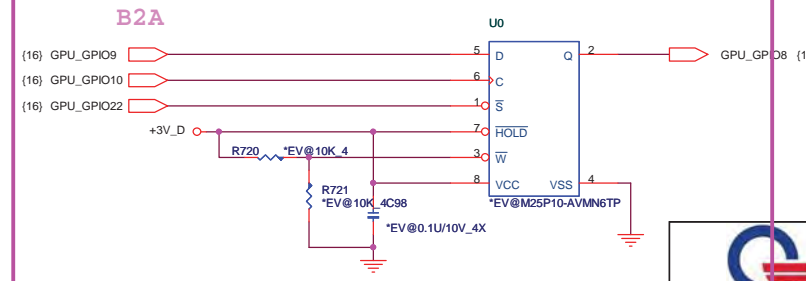
Vendor	Vendor P/N	STN B/S P/N	Size	RAM_STRAP3 DVPDATA_3	RAM_STRAP2 DVPDATA_2	RAM_STRAP1 DVPDATA_1	RAM_STRAP0 DVPDATA_0	RAM_STRAP4	
								15"	14"
Hynix	H5TQ1G63BFR-12C	AKD5LZGTW00 (64M*16)	512MB	0	1	0	0	0	1
			1GB	0	0	0	0	0	1
			2GB	0	0	1	0	0	1
Samsung	K4W1G1646E-HC12	AKD5LGGT502 (64M*16)	512MB	0	1	0	1	0	1
			1GB	0	0	0	1	0	1
	K4W2G1646B-HC12	AKD5MGGT501	2GB	0	0	1	1	0	1



## Thermal Sensor



## EEPROM



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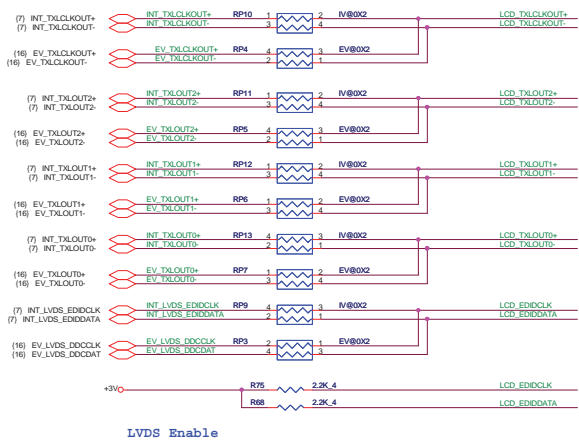
Size: Document Number: Rev: A1A

Memory strip/Thermal/HDCP

Date: Saturday, April 10, 2010 Sheet 22 of 45

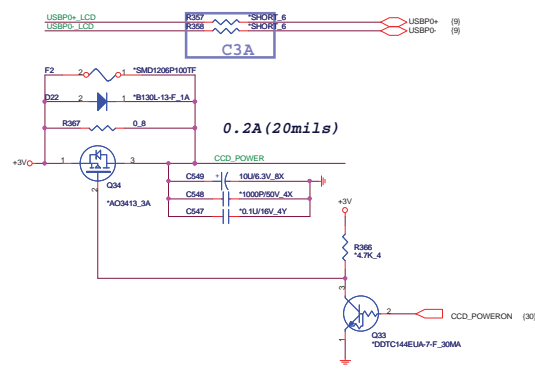


LVDS Signals

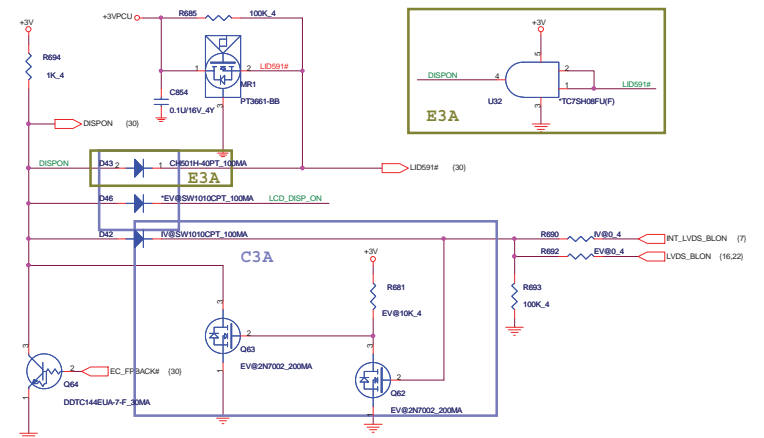


LVDS Enable

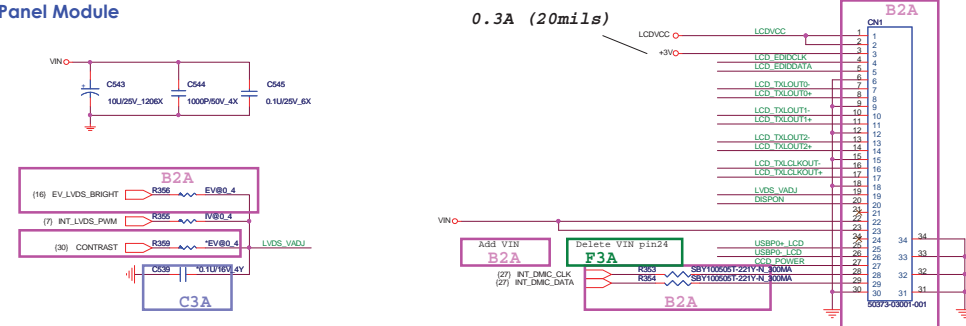
CCD



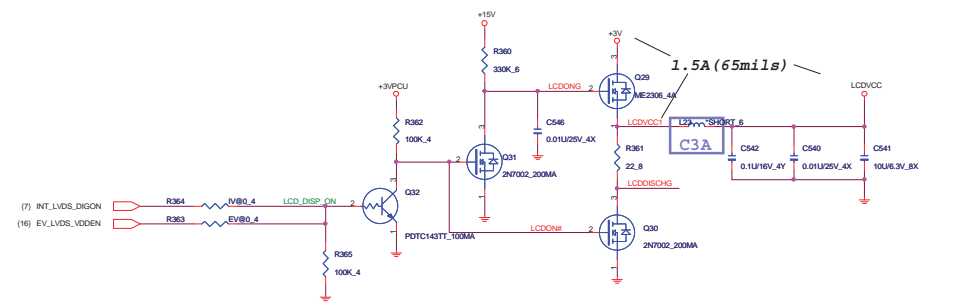
HALL SENSOR&BACK LIGHT SWITCH



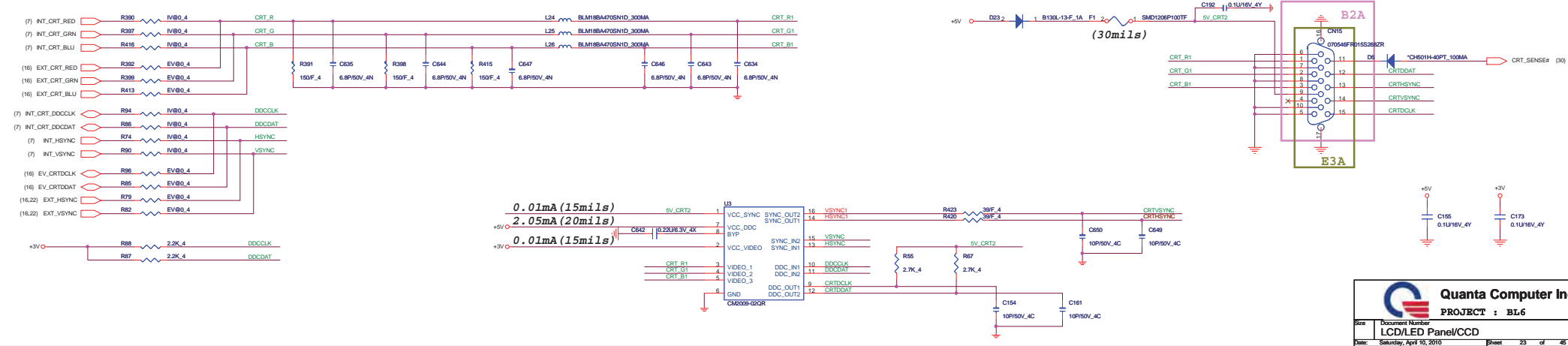
LCD Panel Module



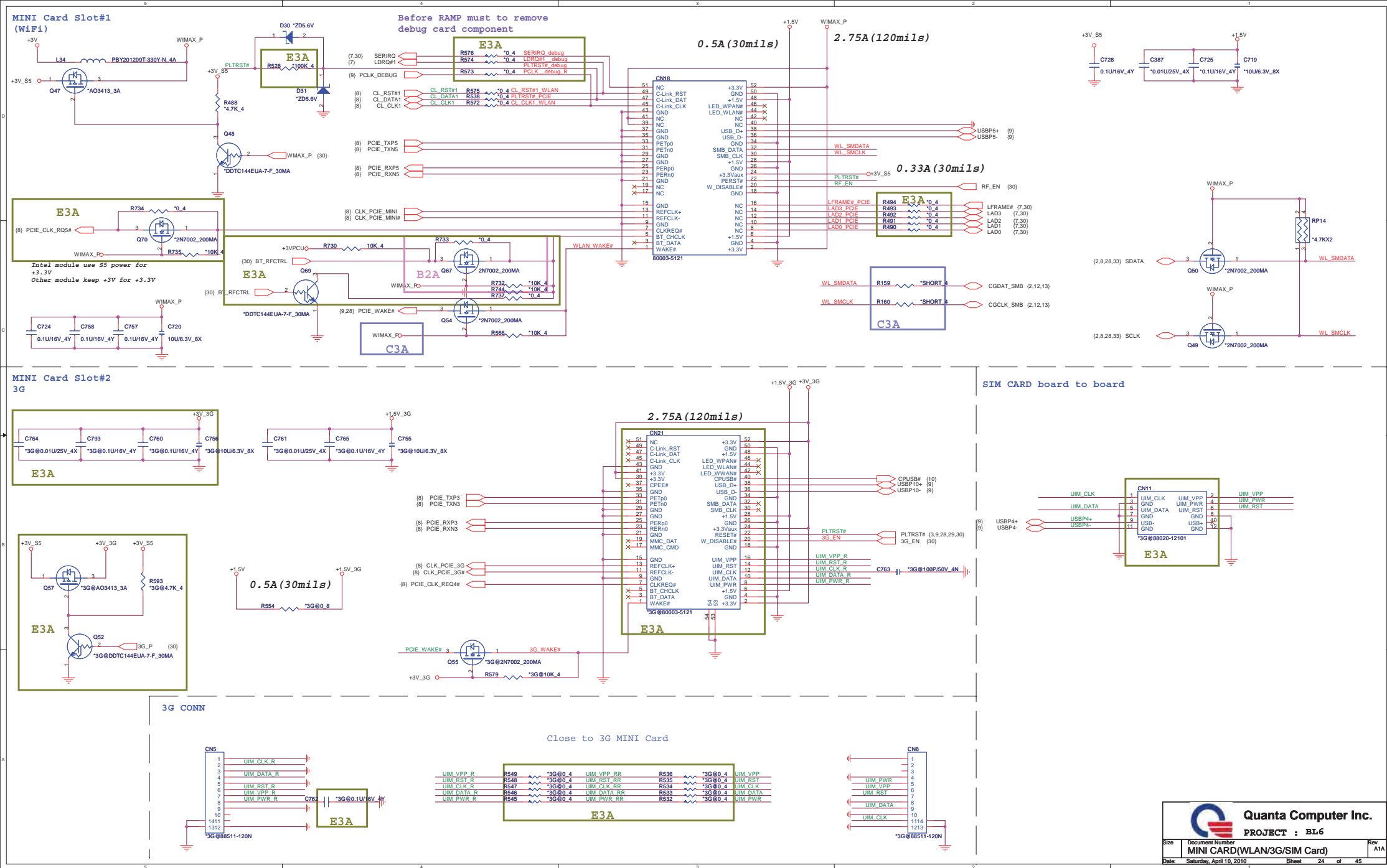
LCD POWER SWITCH



CRT



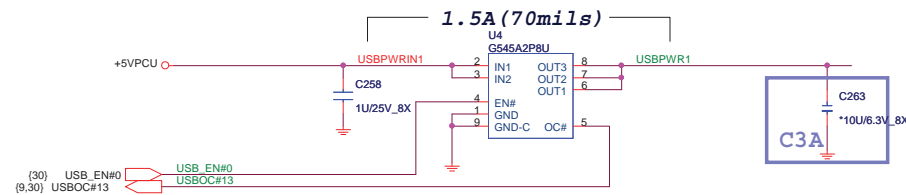
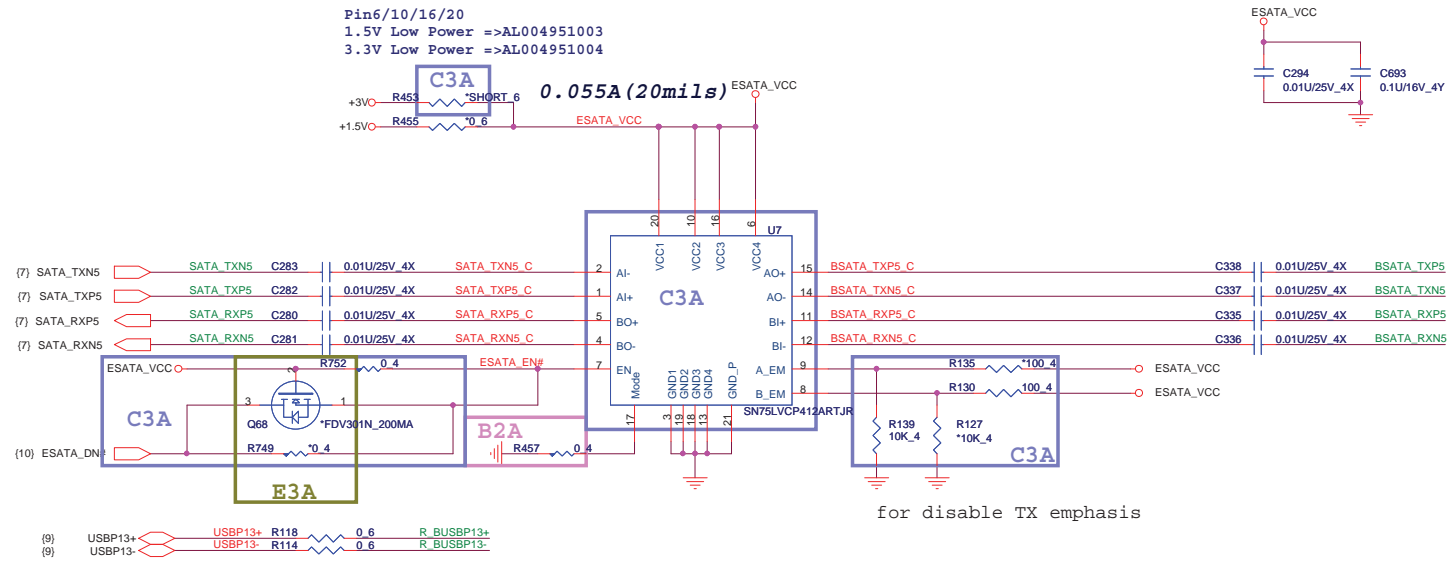




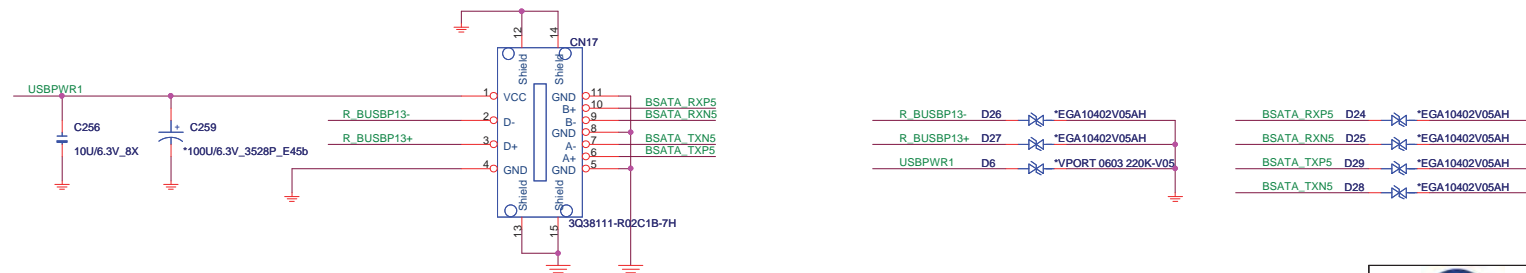


## ESATA Re-driver IC

```
Pin6/10/16/20
1.5V Low Power =>AL004951003
3.3V Low Power =>AL004951004
```

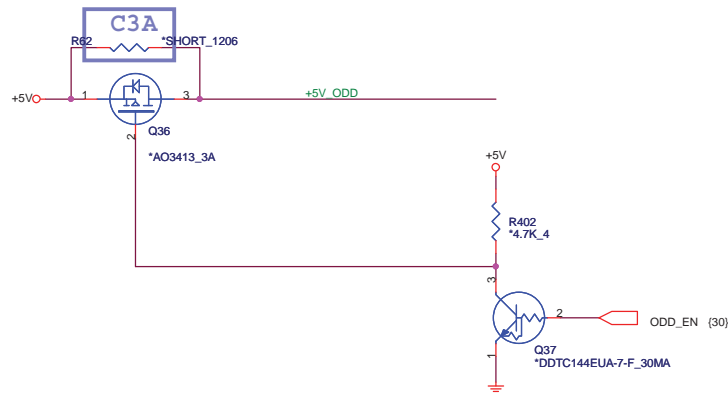
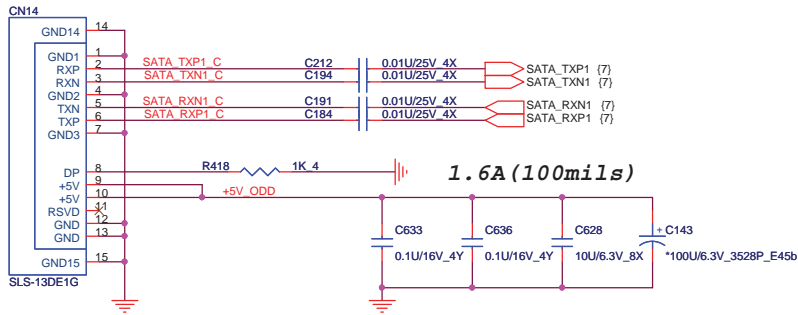


ESATA CONN

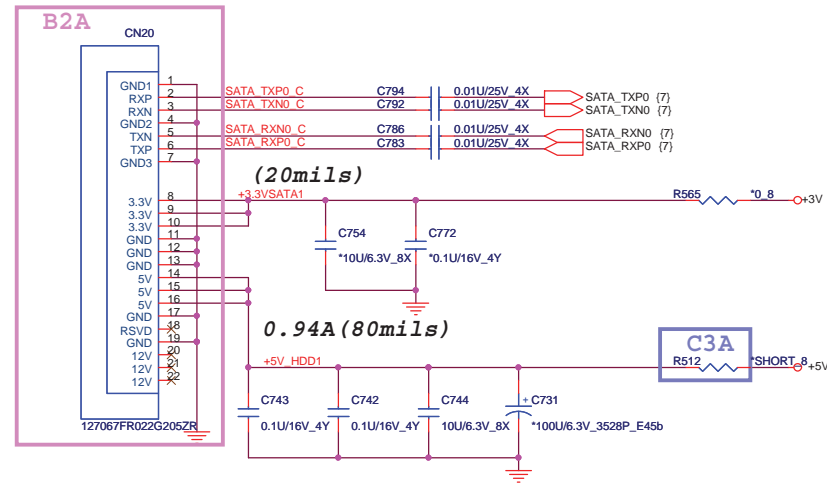




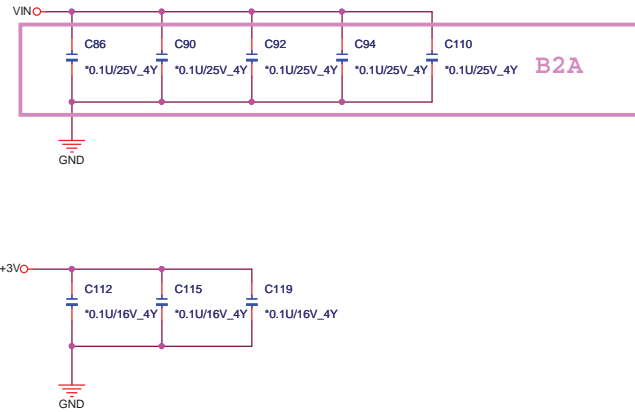
SATA ODD



SATA HDD



EMI





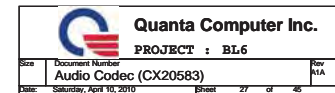
## AUDIO JACKS



## External MIC

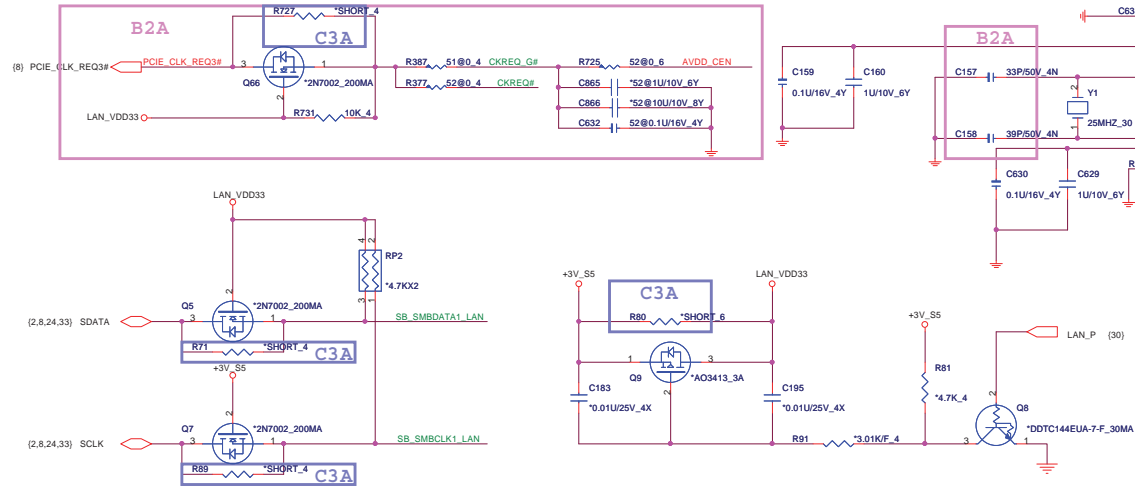
## Internal Speaker

## MDC

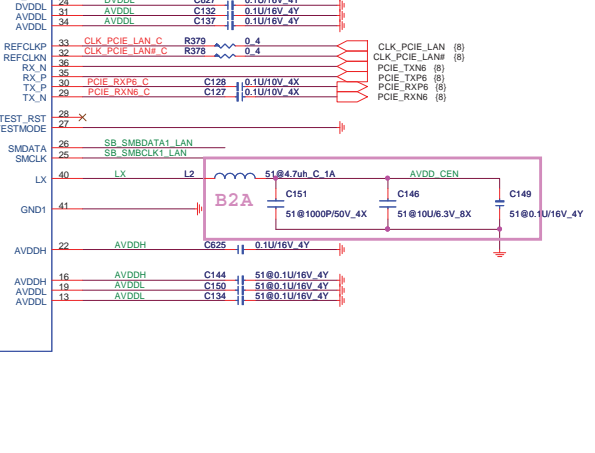
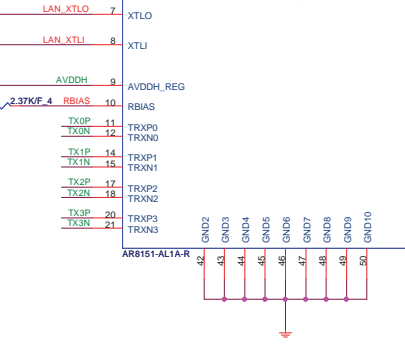




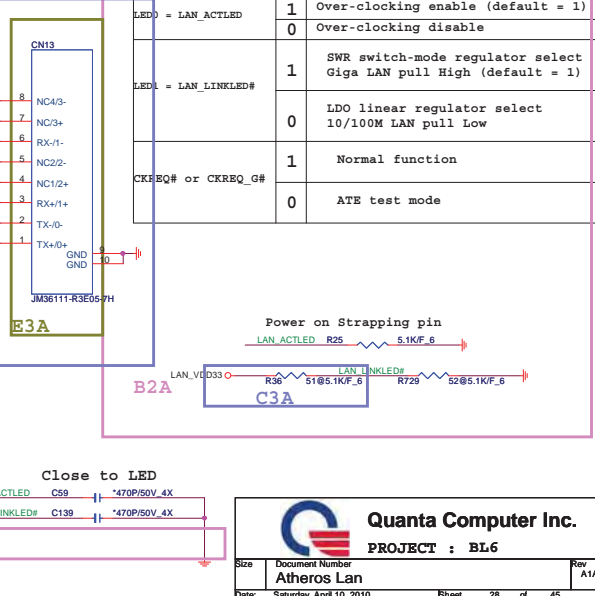
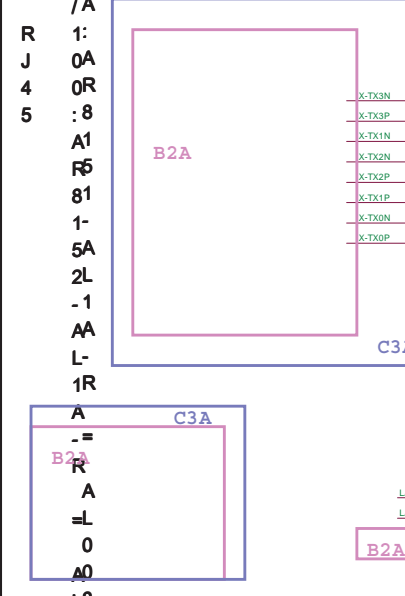
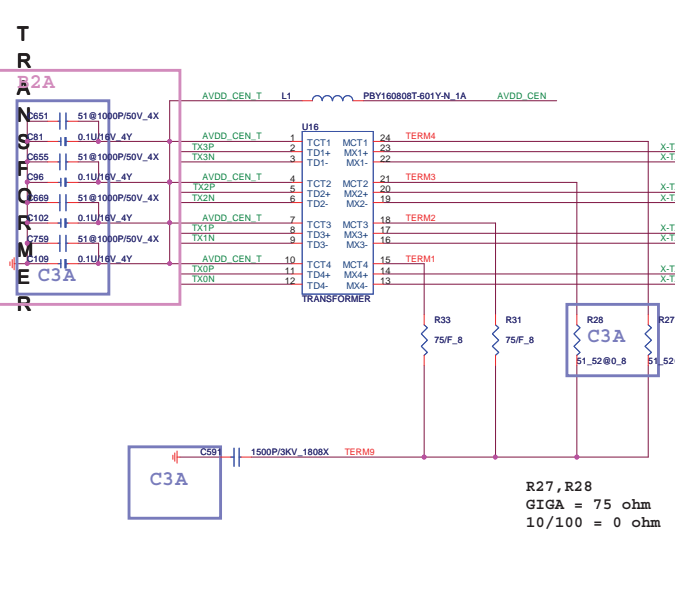
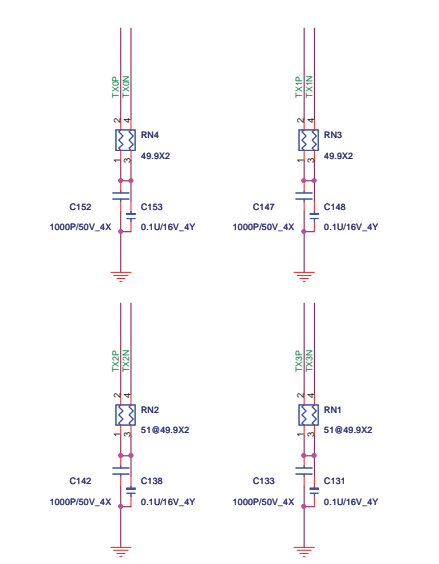
AMD mount Q66, NO mount R727  
INTEL mount R727, No mount Q66



# Atheros AR8151/AR8152

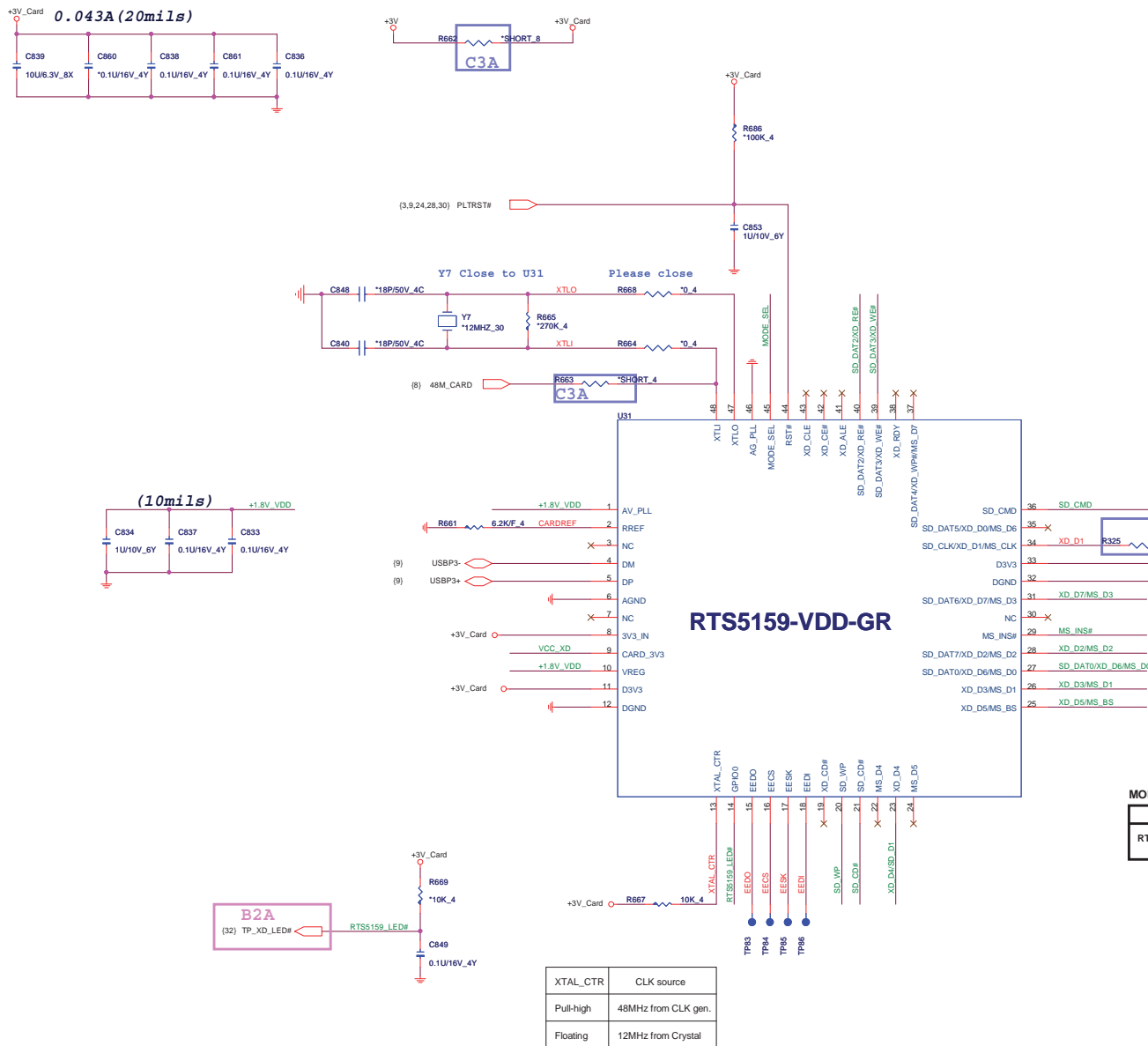


## PLACE NEAR LAN IC SIDE

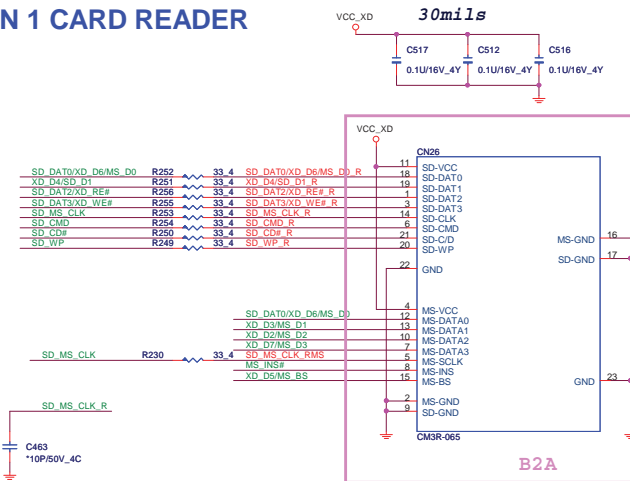




## 5 IN 1 CARD READER



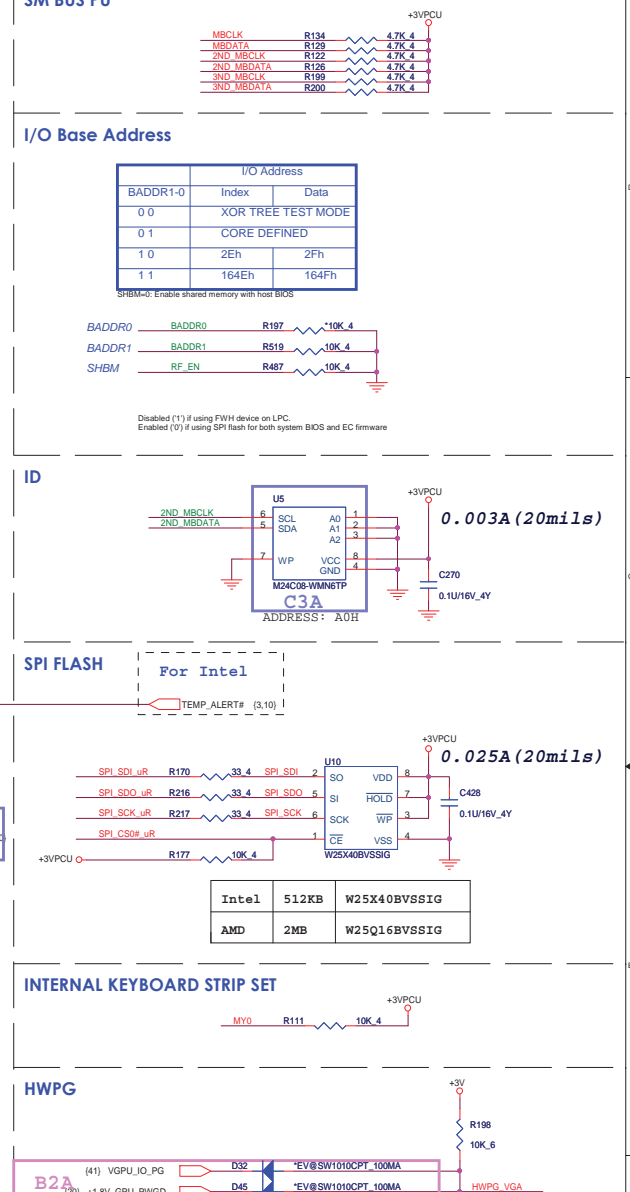
### 3 IN 1 CARD READER



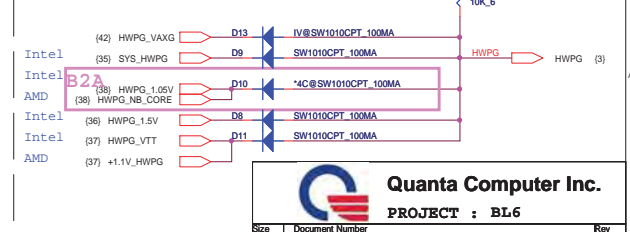
MODE_SEL	R678	C851	Power mode
RTS 5159	0-ohm	NC	USB Auto De-link mode:

XTAL__CTR	CLK source
Pull-high	48MHz from CLK gen.
Floating	12MHz from Crystal





SMBUS	Devices	Address
1	Battery	
2	PCH SML1	
	AMD SMBus	98H
	EC EEPROM	AOH
3	VGA Board Thermal Sensor	98H



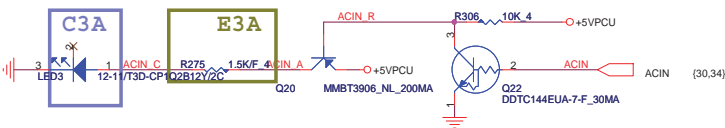




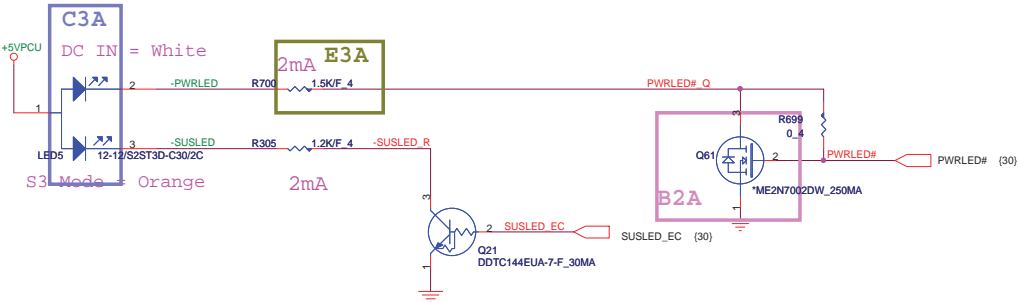


## LED

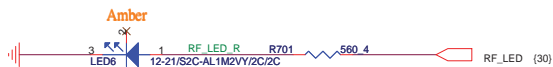
### AC-IN



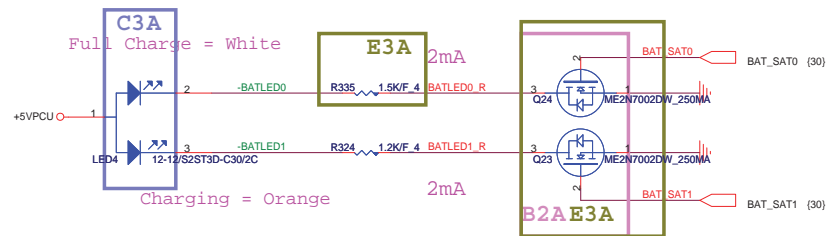
### POWER



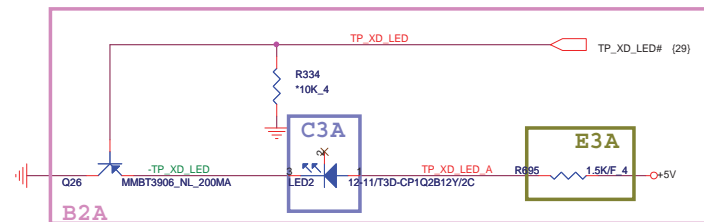
### RF LED



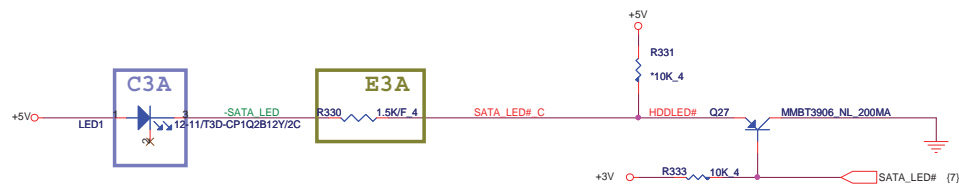
## BATTERY



## CARDREADER

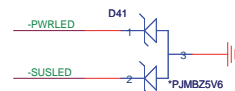


## HDD/ODD

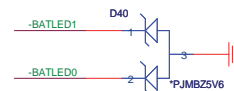


## ESD Protect

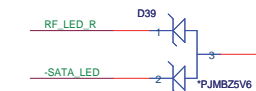
### FOR POWER LED



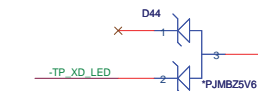
### FOR BATTERY LED



### FOR HDD/RF LED



### FOR CARDREADER LED

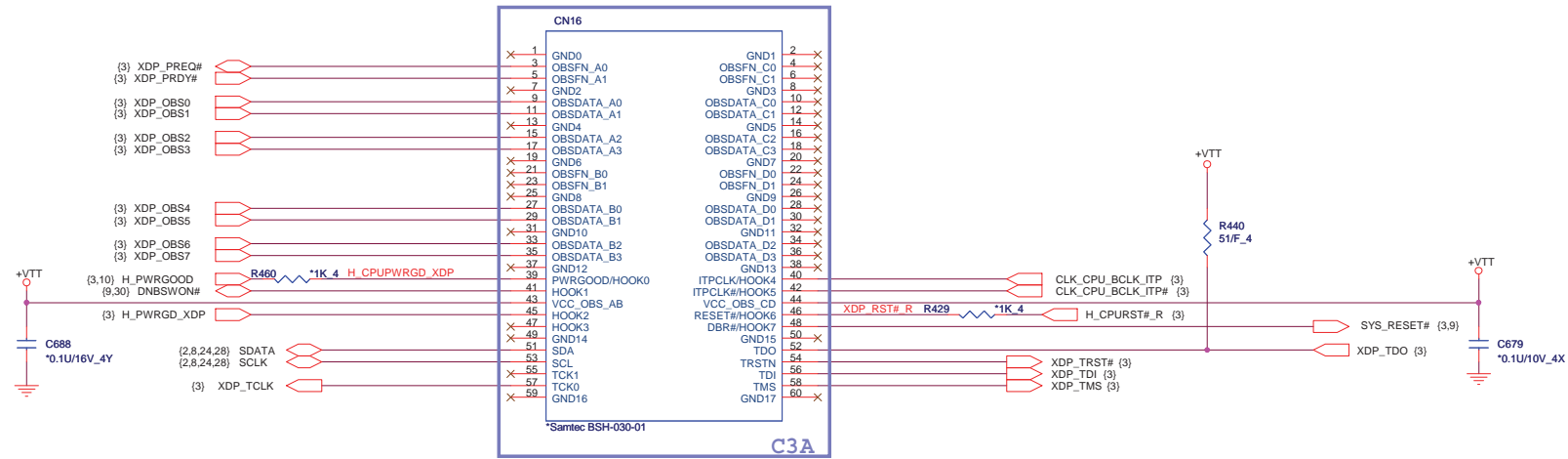


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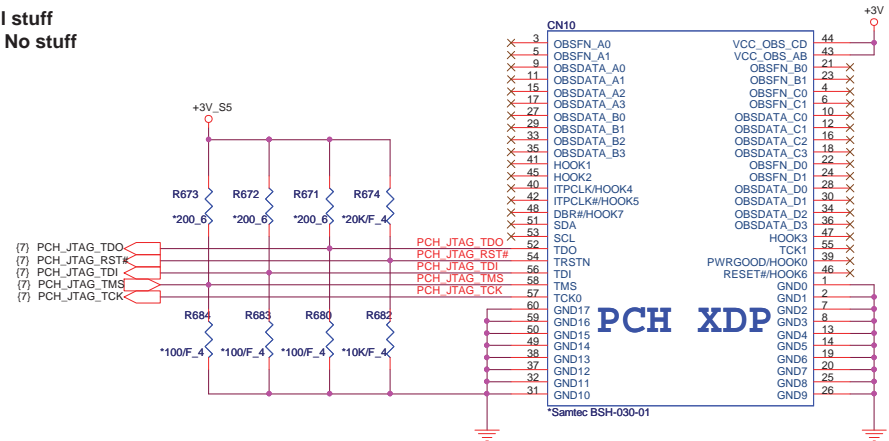
CPU XDP



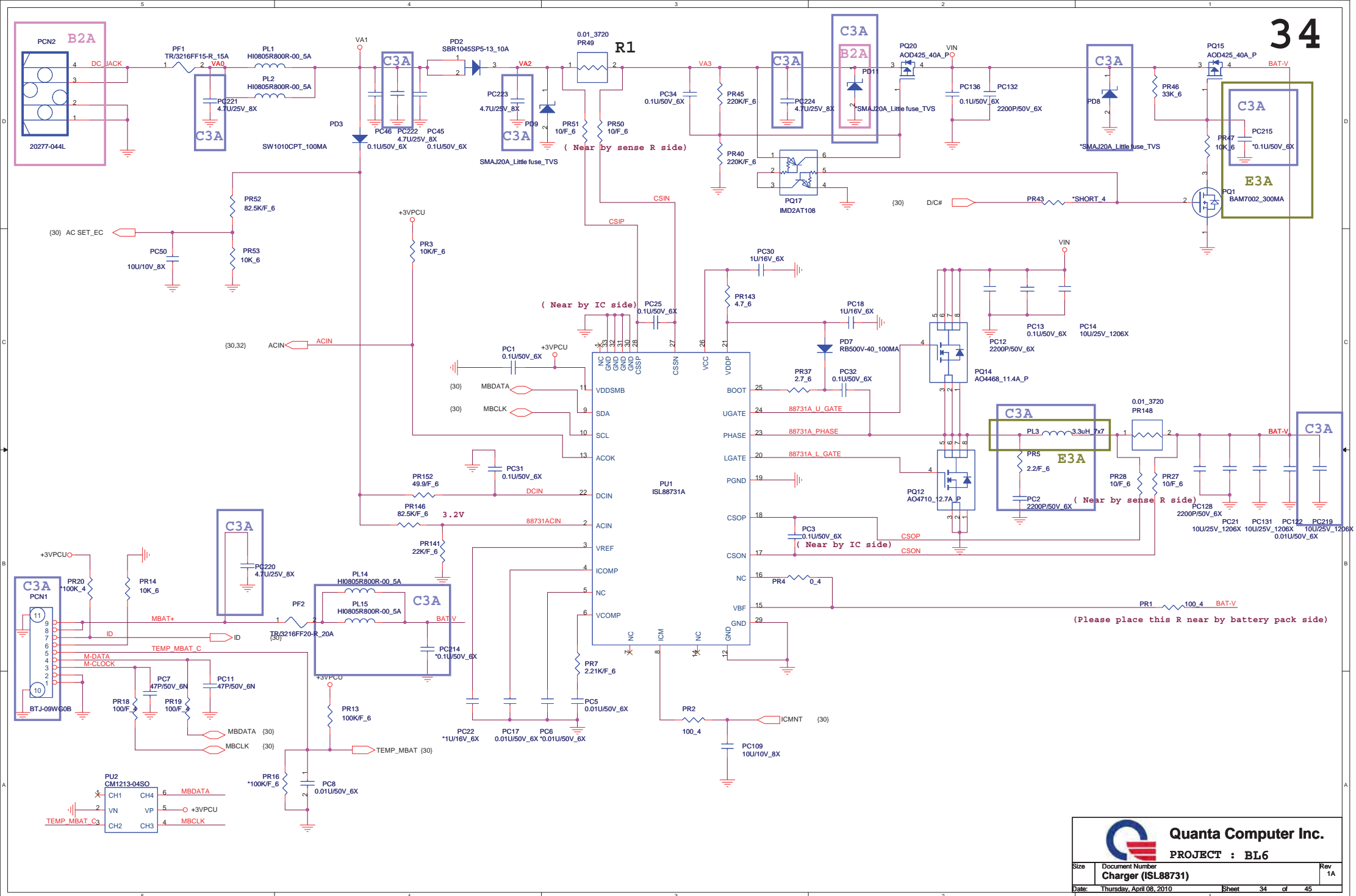
Feature Set	SKU Name (S)				
	Q57	H57	H55	P55	P57
BraidWood	Y	Y	N	N	Y

PCH XDP

Note: For ES1/ES2 version all stuff  
Production version all No stuff



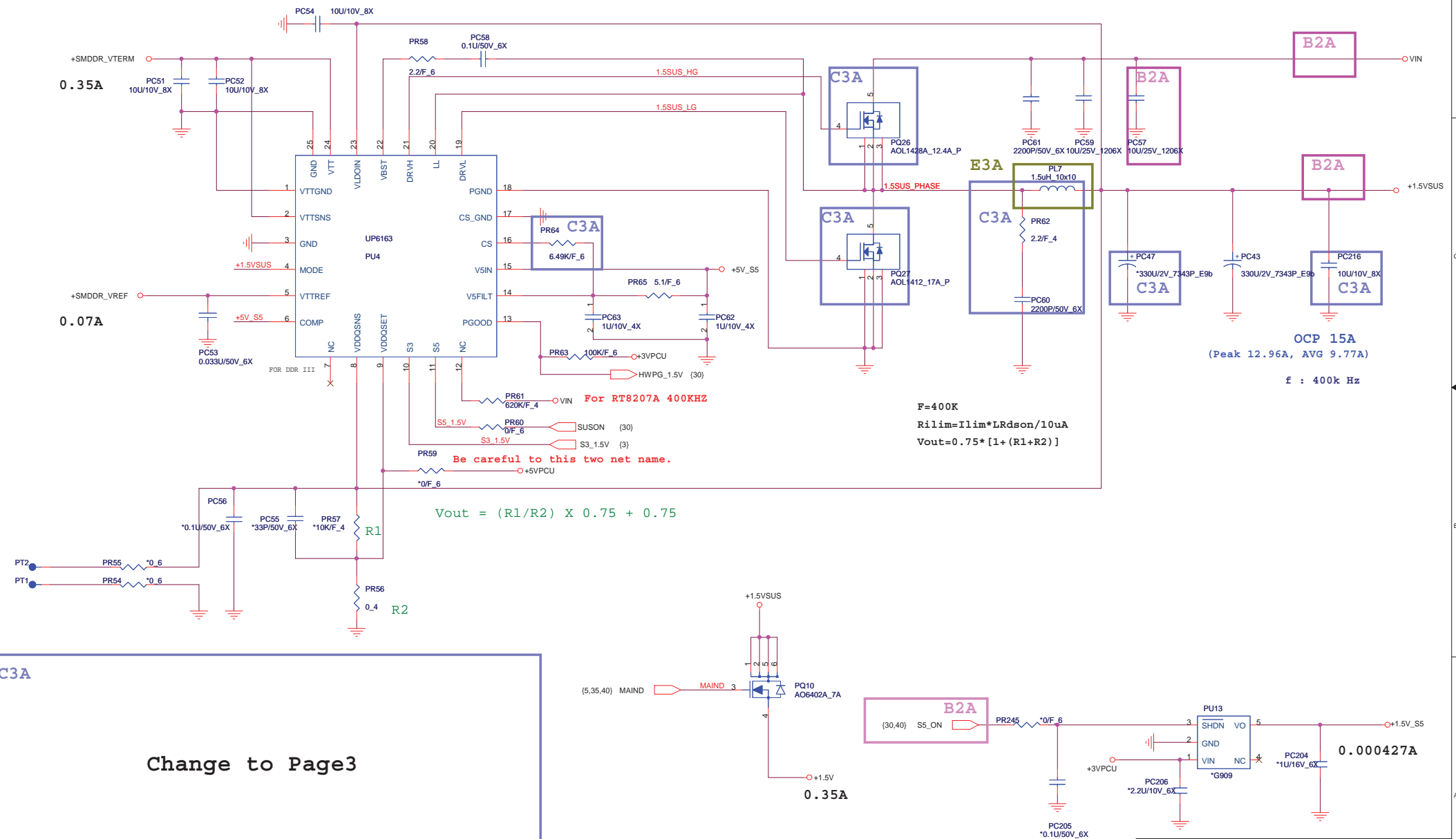








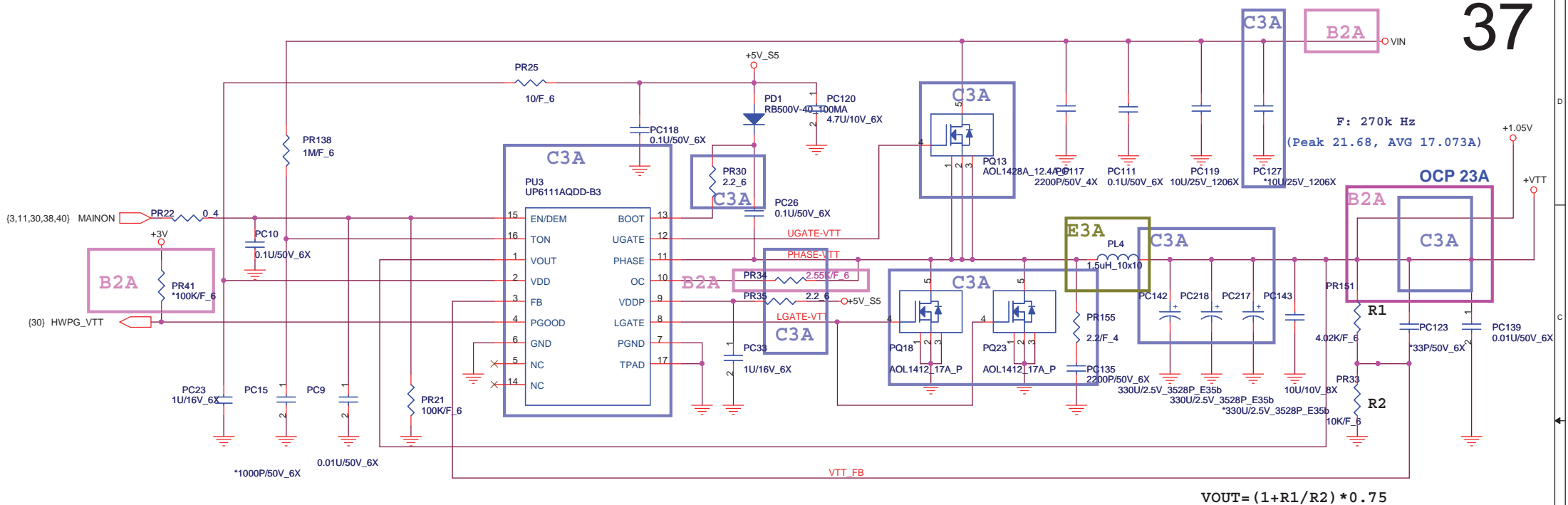




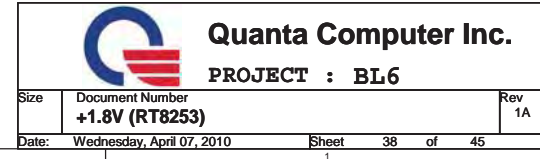
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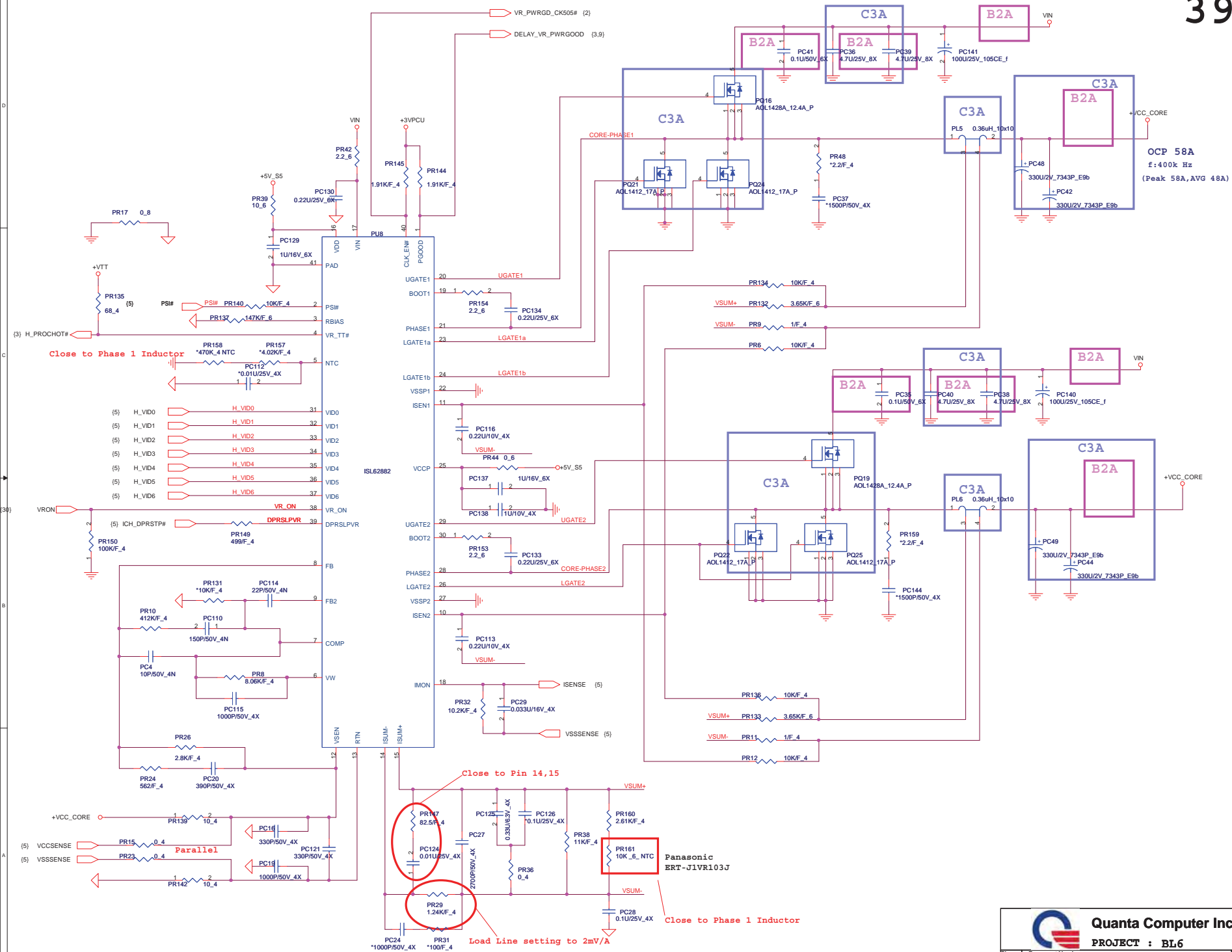




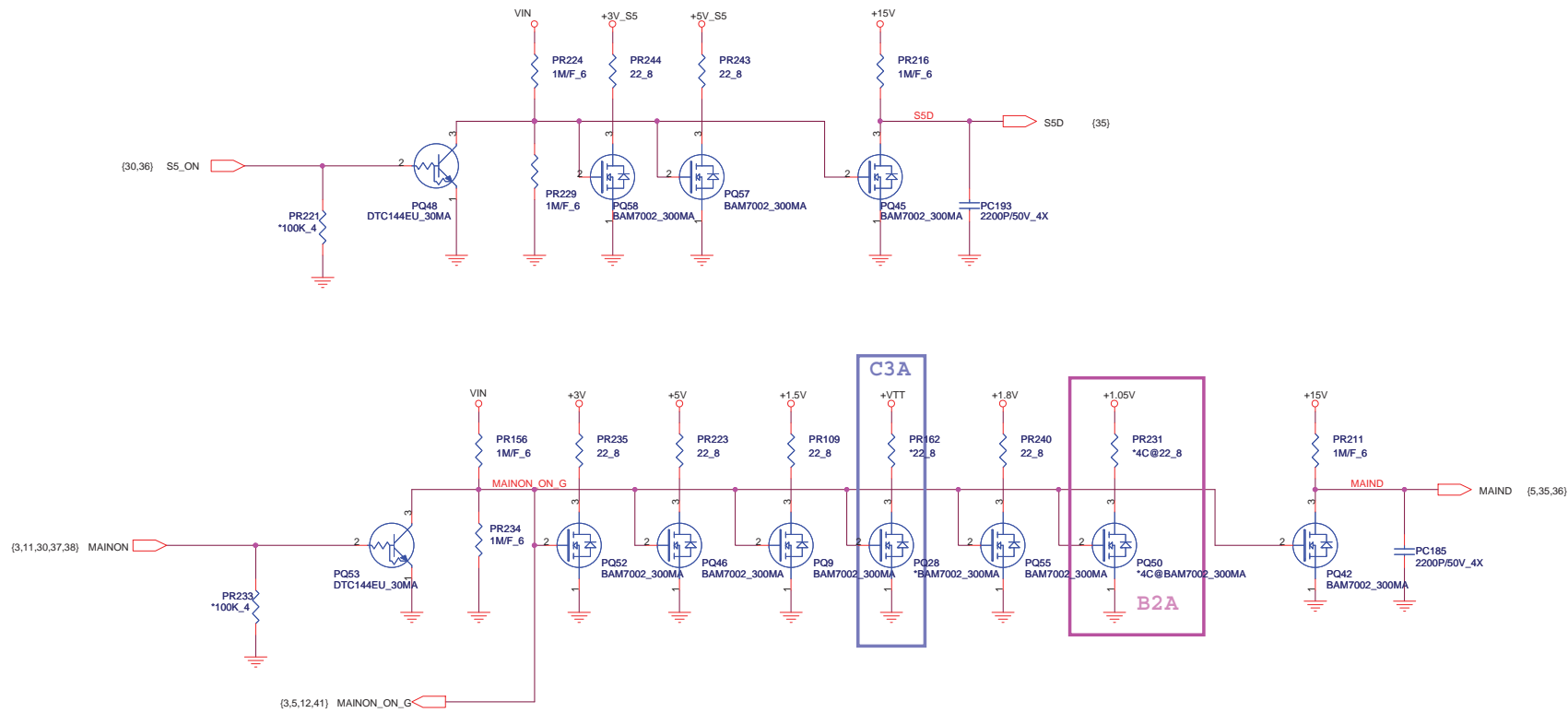




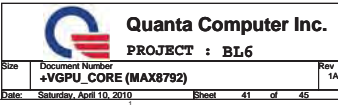




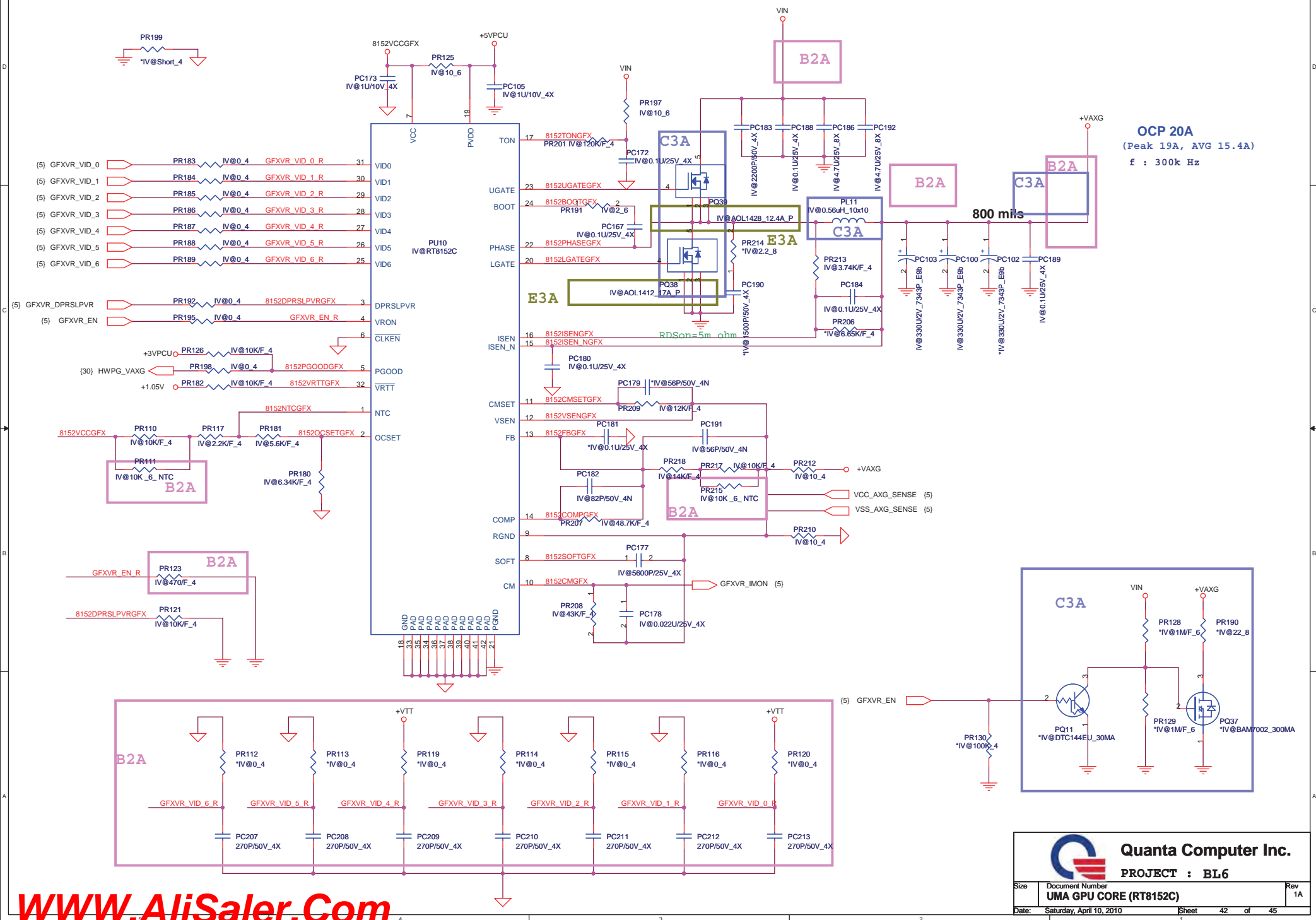






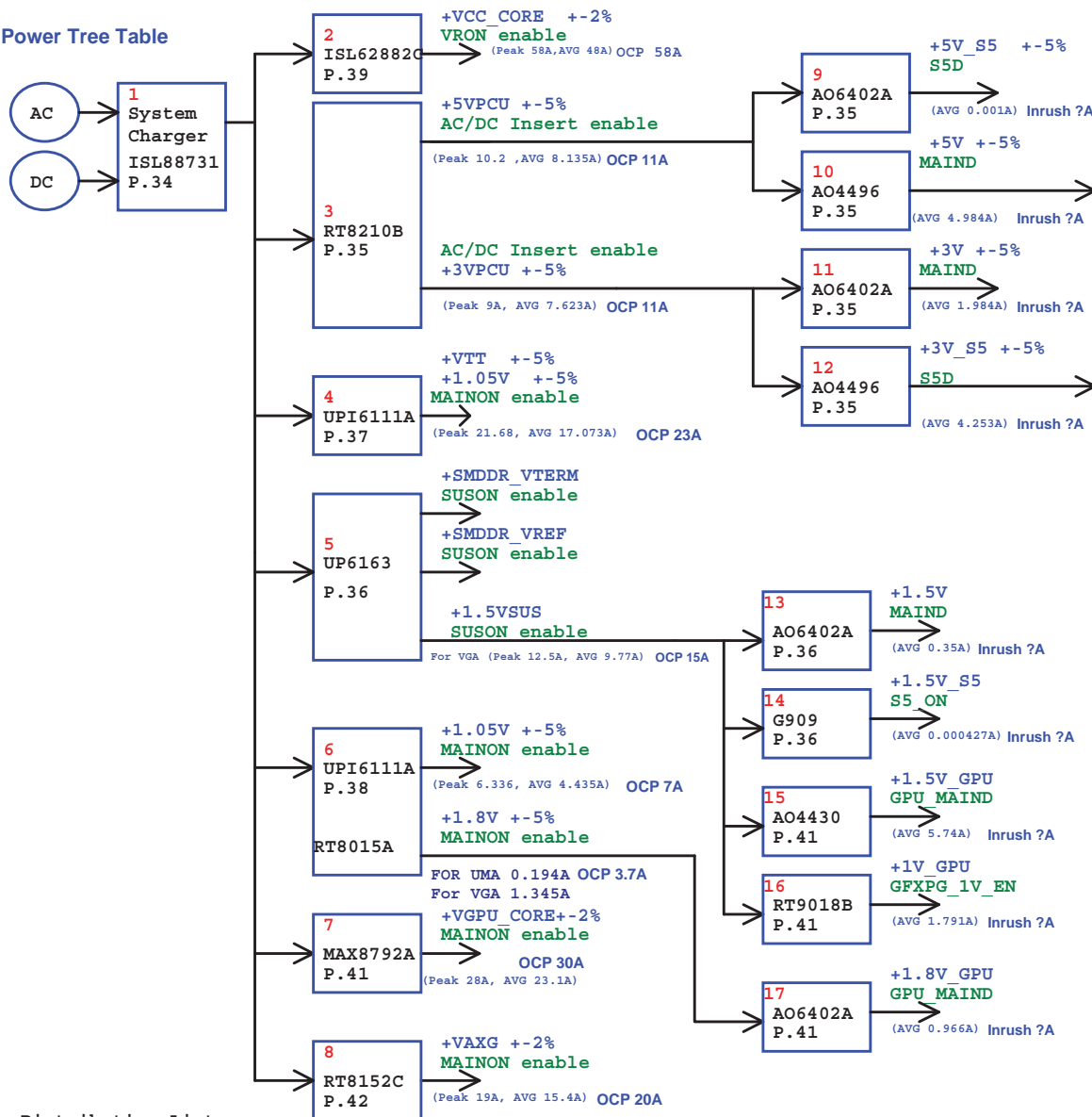








## Power Tree Table



## Power Distribution List

[illegible]